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FACULTY OF ENGINEERING & TECHNOLOGY

CSPS-106 Computer Organization

Lecture-17

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OUTLINE

- INTERRUPT PROCEDURE
- RISC: REDUCED INSTRUCTION SET COMPUTERS
- COMPLEX INSTRUCTION SET COMPUTERS: CISC
- PHYLOSOPHY OF RISC
- CHARACTERISTICS OF RISC

Interrupt Procedure and Subroutine Call

- The interrupt is usually initiated by an internal or an external signal rather than from the execution of an instruction (except for the software interrupt)
- The address of the interrupt service program is determined by the hardware rather than from the address field of an instruction
- An interrupt procedure usually stores all the information necessary to define the state of CPU rather than storing only the PC.

The state of the CPU is determined from;

Content of the PC

Content of all processor registers

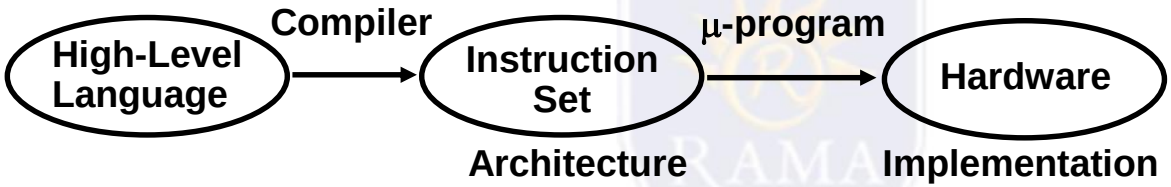
Content of status bits

Many ways of saving the CPU state depending on the CPU architectures

Historical Background

IBM System/360, 1964

- The real beginning of modern computer architecture
- Distinction between *Architecture* and *Implementation*
- Architecture: The abstract structure of a computer seen by an assembly-language programmer



Continuing growth in semiconductor memory and microprogramming
-> A much richer and complicated instruction sets
=> CISC(Complex Instruction Set Computer)

- Arguments advanced at that time
  - Richer instruction sets would simplify compilers
  - Richer instruction sets would alleviate the software crisis
    - move as much functions to the hardware as possible
    - close *Semantic Gap* between machine language and the high-level language
  - Richer instruction sets would improve the *architecture quality*

COMPLEX INSTRUCTION SET COMPUTERS: CISC

High Performance General Purpose Instructions

Characteristics of CISC:

1. A large number of instructions (from 100-250 usually)
2. Some instructions that performs a certain tasks are not used frequently.
3. Many addressing modes are used (5 to 20)
4. Variable length instruction format.
5. Instructions that manipulate operands in memory.

PHYLOSOPHY OF RISC

Reduce the semantic gap between

machine instruction and microinstruction

1-Cycle instruction

Most of the instructions complete their execution

in 1 CPU clock cycle - like a microoperation

* Functions of the instruction (contrast to CISC)

- Very simple functions

- Very simple instruction format

- Similar to microinstructions

=> No need for microprogrammed control

PHYLOSOPHY OF RISC

***** Register-Register Instructions

- Avoid memory reference instructions except Load and Store instructions
- Most of the operands can be found in the registers instead of main memory

=> Shorter instructions

=> Uniform instruction cycle

=> Requirement of large number of registers

* Employ instruction pipeline

CHARACTERISTICS OF RISC

Common RISC Characteristics

- Operations are register-to-register, with only LOAD and STORE accessing memory

- The operations and addressing modes are reduced

  Instruction formats are simple

CHARACTERISTICS OF RISC

RISC Characteristics

- Relatively few instructions

- Relatively few addressing modes

- Memory access limited to load and store instructions

- All operations done within the registers of the CPU

- Fixed-length, easily decoded instruction format

- Single-cycle instruction format

- Hardwired rather than microprogrammed control

CHARACTERISTICS OF RISC

More RISC Characteristics

-**A relatively large numbers of registers in the processor unit.**

-**Efficient instruction pipeline**

-**Compiler support: provides efficient translation of high-level language programs into machine language programs.**

Advantages of RISC

- VLSI Realization

- Computing Speed

- Design Costs and Reliability

- High Level Language Support

Multiple Choice Question

MUTIPLE CHOICE QUESTIONS:

Sr no	Question	Option A	Option B	OptionC	OptionD
1	Process of replacing the sequence of lines of codes is knownas	Expanding diemacro	Expanding trimacro	Tetramacro	None ofthese
2	A program that links several programs is called	Linker	Loader	Translator	None ofthese
3	address is not assigned bylinker:	Absolute	Relative	Both a &b	None ofthese
4	_____address is provided by linker to modules linked together thatstartingfrom :	Absolute and0	Relative and0	Relative and1	Relative and3
5	A linker is also knownas	Binder	Linkageeditor	Both a &b	None ofthese

REFERENCES

- http://www.engppt.com/search/label/Computer%20Organization%20and%20Architecture
- http://www.engppt.com/search/label/Computer%20Architecture%20ppt