RAMA UNIVERSITY

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FACULTY OF ENGINEERING & TECHNOLOGY

CSPS-106 Computer Organization

Lecture-02

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OUTLINE

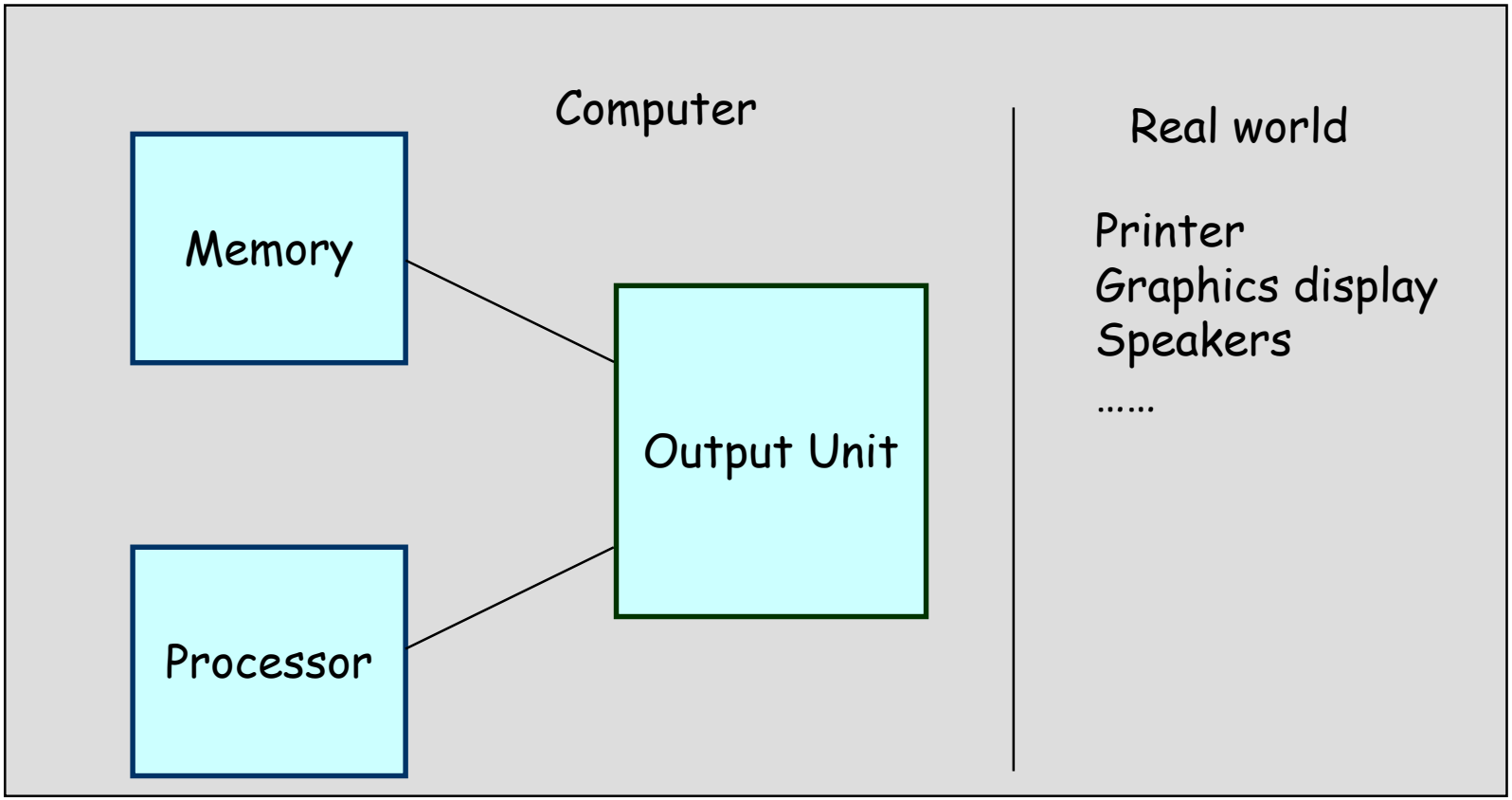
- ARITHMETIC AND LOGIC UNIT (ALU)
- OUTPUT UNIT
- CONTROL UNIT
- HOW ARE THE FUNCTIONAL UNITS CONNECTED?
- ORGANIZATION OF CACHE AND MAIN MEMORY UNIT

ARITHMETIC AND LOGIC UNIT (ALU)

- Operations are executed in the Arithmetic and Logic Unit (ALU).
  - Arithmetic operations such as addition, subtraction.
  - Logic operations such as comparison of numbers.
- In order to execute an instruction, operands need to be brought into the ALU from the memory.
  - Operands are stored in general purpose registers available in the ALU.
  - Access times of general purpose registers are faster than the cache.
- Results of the operations are stored back in the memory or retained in the processor for immediate use.

OUTPUT UNIT

•Computers represent information in a specific binary form. Output units:
- Interface with output devices.
- Accept processed results provided by the computer in specific binary form.
- Convert the information in binary form to a form understood by an output device.



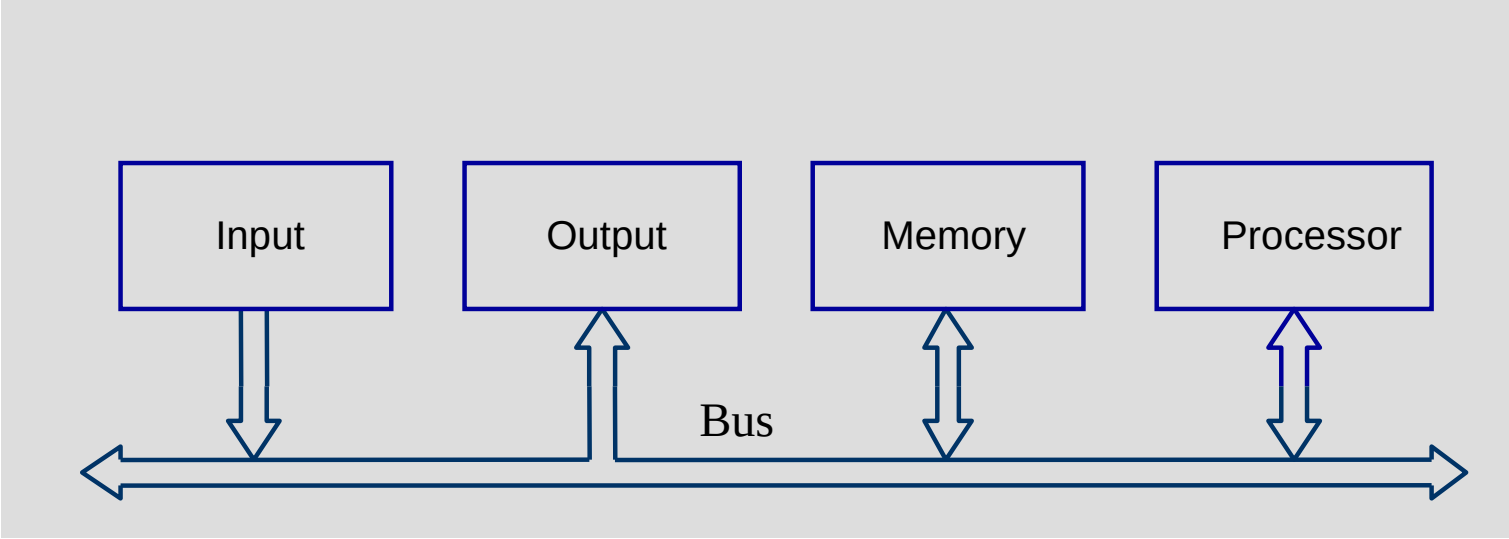
CONTROL UNIT

- Operation of a computer can be summarized as:
  - Accepts information from the input units (Input unit).
  - Stores the information (Memory).
  - Processes the information (ALU).
  - Provides processed results through the output units (Output unit).
- Operations of Input unit, Memory, ALU and Output unit are coordinated by Control unit.
- Instructions control “what” operations take place (e.g. data transfer, processing).
- Control unit generates timing signals which determines “when” a particular operation takes place.

HOW ARE THE FUNCTIONAL UNITS CONNECTED?

•For a computer to achieve its operation, the functional units need to communicate with each other.

•In order to communicate, they need to be connected.



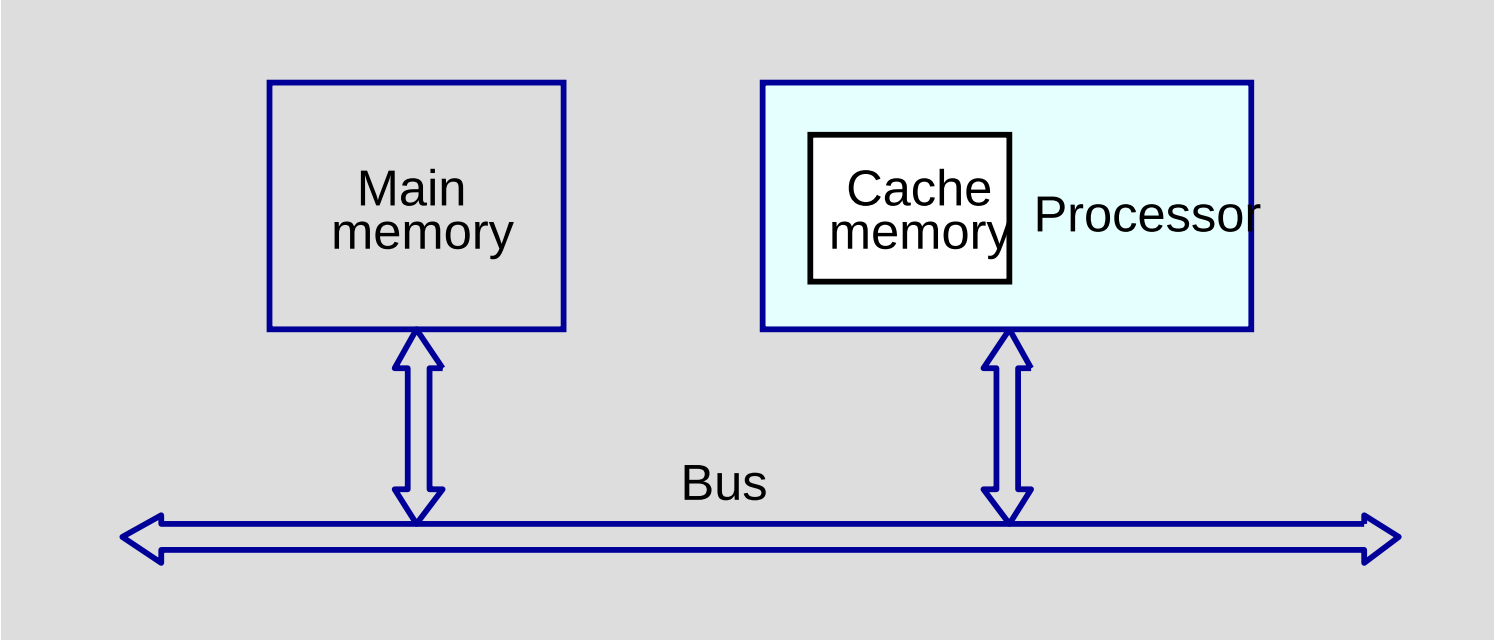
•Functional units may be connected by a group of parallel wires.

•The group of parallel wires is called a bus.

•Each wire in a bus can transfer one bit of information.

•The number of parallel wires in a bus is equal to the word length of a computer

ORGANIZATION OF CACHE AND MAIN MEMORY



Why is the access time of the cache memory lesser than the access time of the main memory?

Multiple Choice Question

MUTIPLE CHOICE QUESTIONS:

Sr no	Question	Option A	Option B	OptionC	OptionD
1	_____ are numbers and encoded characters, generally used as operands.	Input	Data	information	story value
2	_____ bus structure is usually used to connect I/O devices.	multiple bus	star bus	single bus	Ram bus
3	. To reduce the memory access time we generally make use of _____	SD RAM	dynamic ram	heaps	cache
4	The control unit controls other units by generating _____	Control signals	Timing signals	Transfer signals	all of above
5	The Input devices can send information to the processor.	When the SIN status flag is set	When the data arrives regardless of the SIN flag	Neither of the cases	Either of the cases

REFERENCES

- http://www.engppt.com/search/label/Computer%20Organization%20and%20Architecture
- http://www.engppt.com/search/label/Computer%20Architecture%20ppt