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FACULTY OF ENGINEERING & TECHNOLOGY

CSPS-106 Computer Organization

Lecture-08

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OUTLINE

- ENIAC – BACKGROUND
- STRUCTURE OF VON NEUMANN MACHINE
- STRUCTURE OF IAS
- GENERATIONS OF COMPUTER
- PENTIUM EVOLUTION

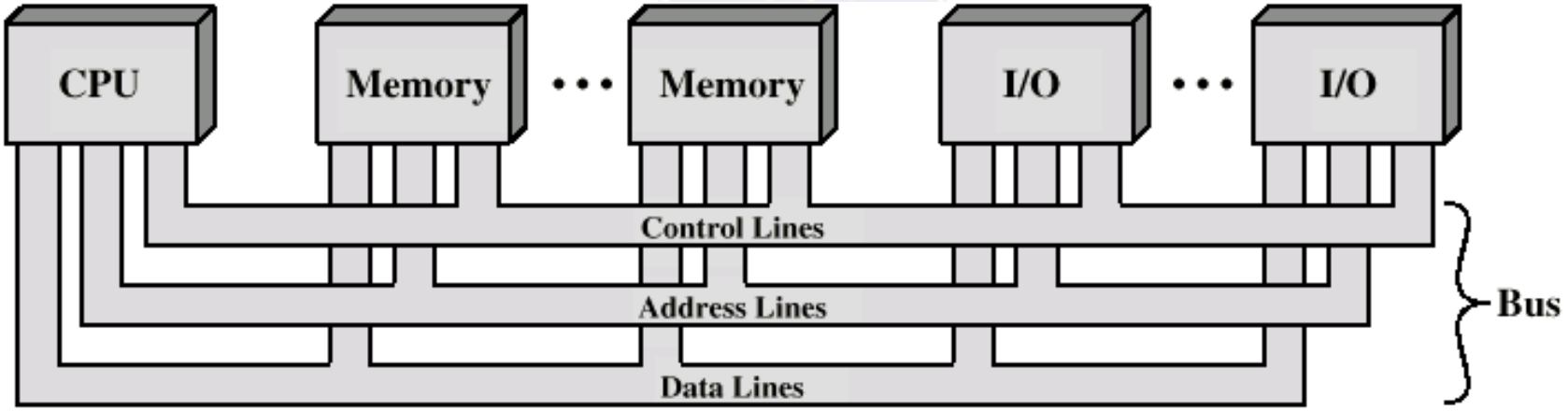
BUSES

- There are a number of possible interconnection systems
- Single and multiple BUS structures are most common
- e.g. Control/Address/Data bus (PC)
- e.g. Unibus (DEC-PDP)

WHAT IS A BUS?

- A communication pathway connecting two or more devices
- Usually broadcast (all components see signal)
- Often grouped
  - A number of channels in one bus
  - e.g. 32 bit data bus is 32 separate single bit channels
- Power lines may not be shown

BUS INTERCONNECTION SCHEME



DATA BUS

- Carries data
  - Remember that there is no difference between “data” and “instruction” at this level
- Width is a key determinant of performance
  - 8, 16, 32, 64 bit

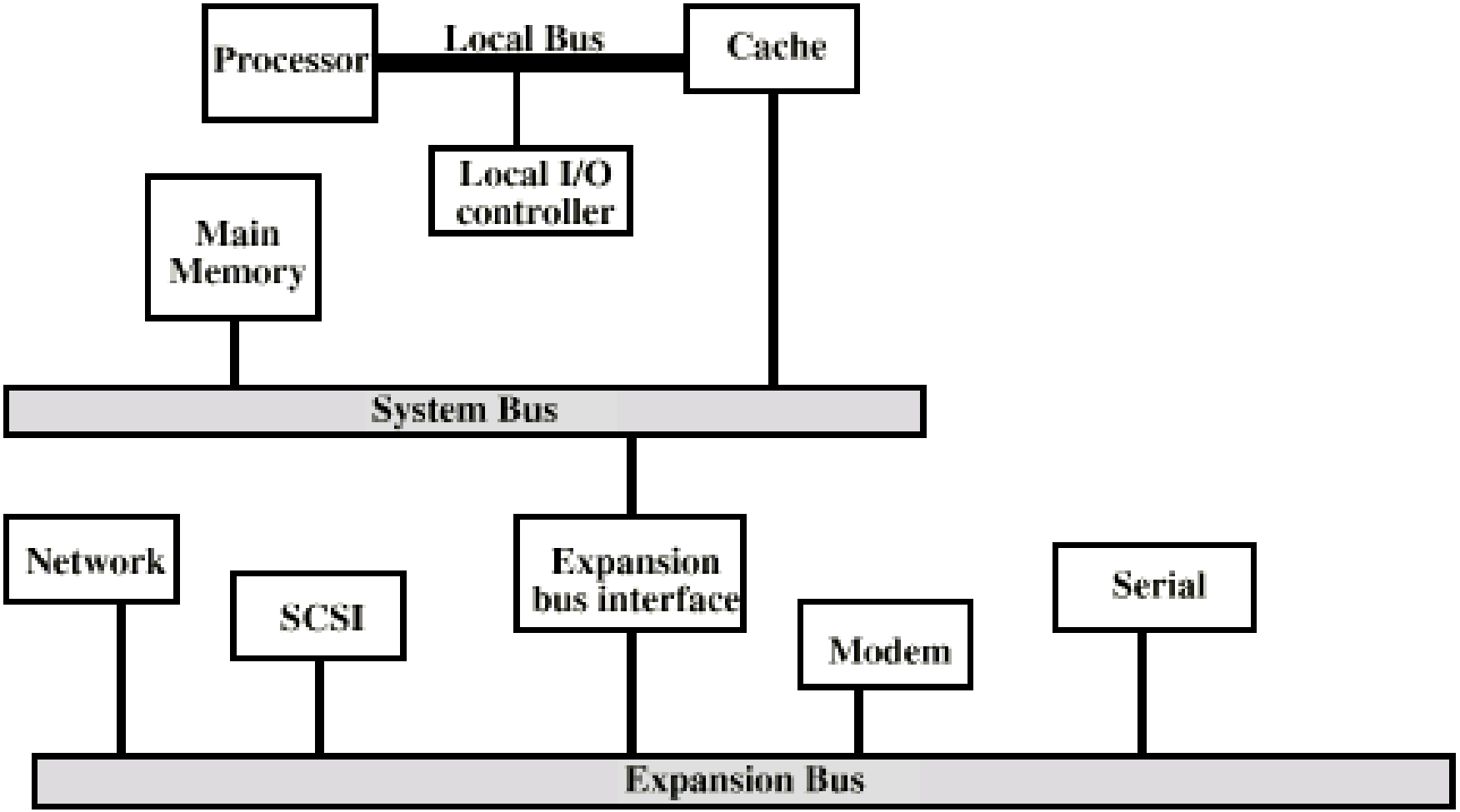
ADDRESS BUS

- Identify the source or destination of data
- e.g. CPU needs to read an instruction (data) from a given location in memory
- Bus width determines maximum memory capacity of system
  - e.g. 8080 has 16 bit address bus giving 64k address space

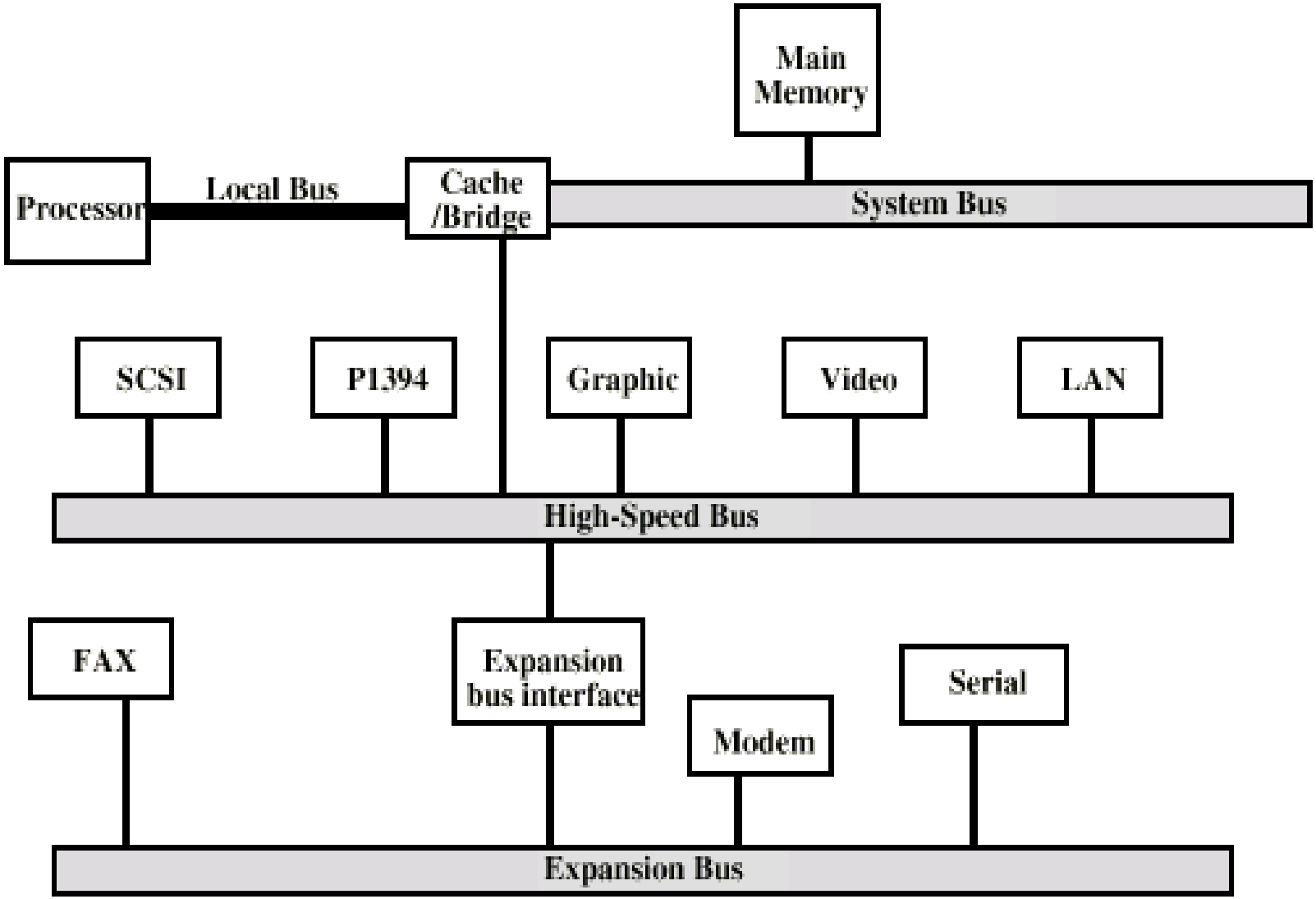
CONTROL BUS

- Control and timing information
  - Memory read/write signal
  - Interrupt request
  - Clock signals

TRADITIONAL (ISA) (WITH CACHE)



HIGH PERFORMANCE BUS



BUS TYPES

- Dedicated
  - Separate data & address lines
- Multiplexed
  - Shared lines
  - Address valid or data valid control line
  - Advantage - fewer lines
  - Disadvantages
    - More complex control
    - Ultimate performance

BUS ARBITRATION

- More than one module controlling the bus
  - e.g. CPU and DMA controller
- Only one module may control bus at one time
- Arbitration may be centralised or distributed

CENTRALISED ARBITRATION

- Single hardware device controlling bus access
  - Bus Controller
  - Arbiter
- May be part of CPU or separate

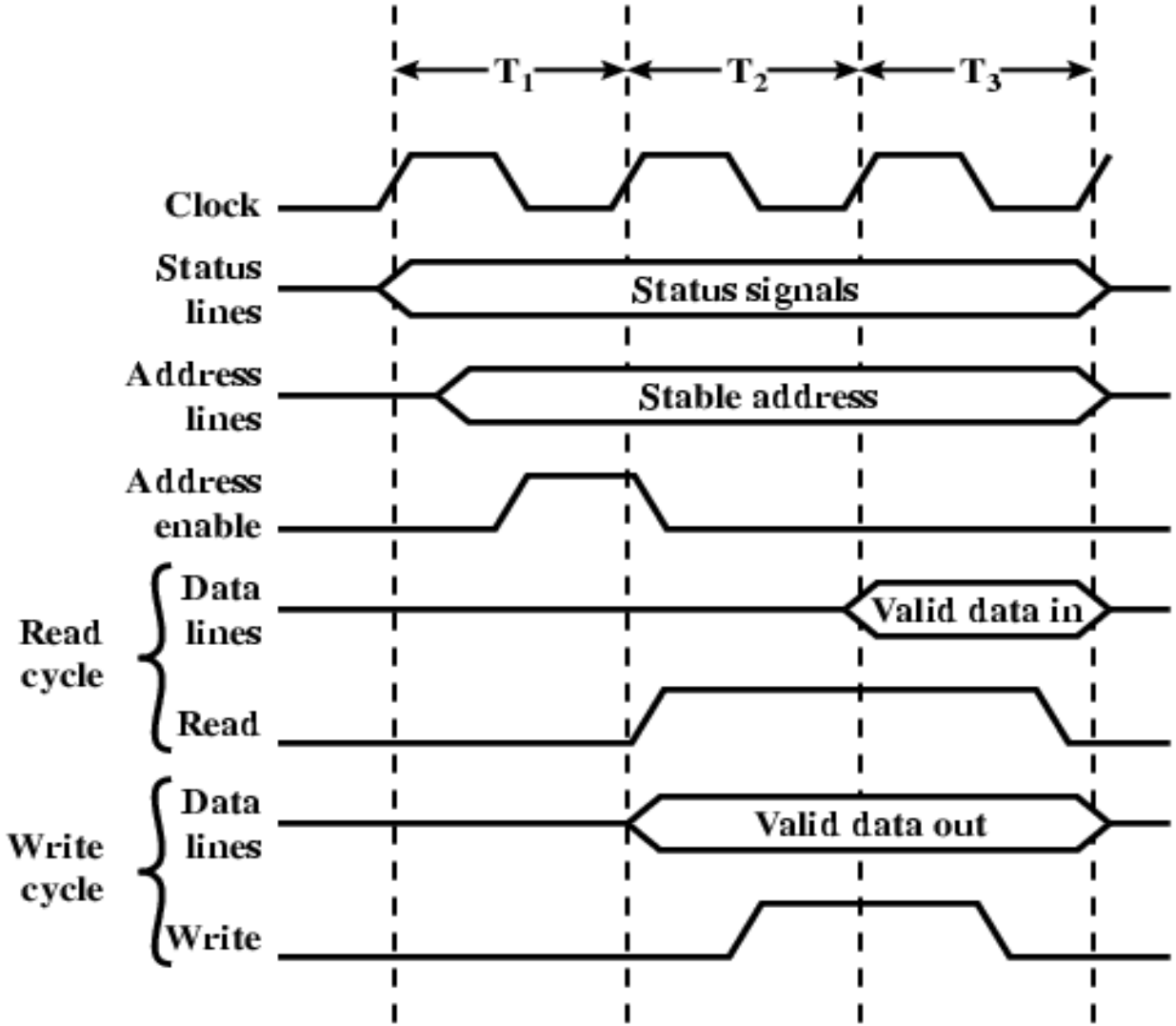
DISTRIBUTED ARBITRATION

- Each module may claim the bus
- Control logic on all modules

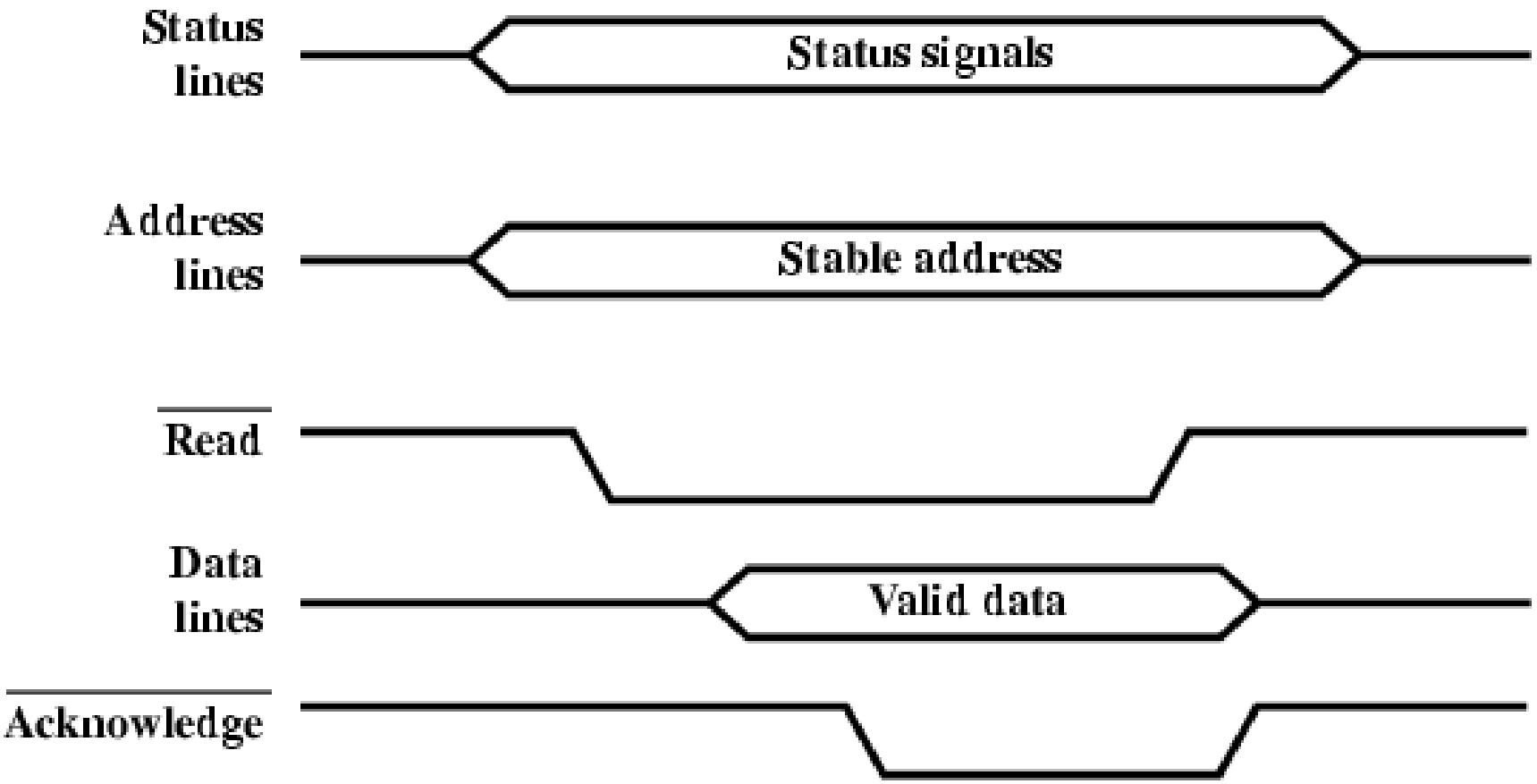
Timing

- Co-ordination of events on bus
- Synchronous
  - Events determined by clock signals
  - Control Bus includes clock line
  - A single 1-0 is a bus cycle
  - All devices can read clock line
  - Usually sync on leading edge
  - Usually a single cycle for an event

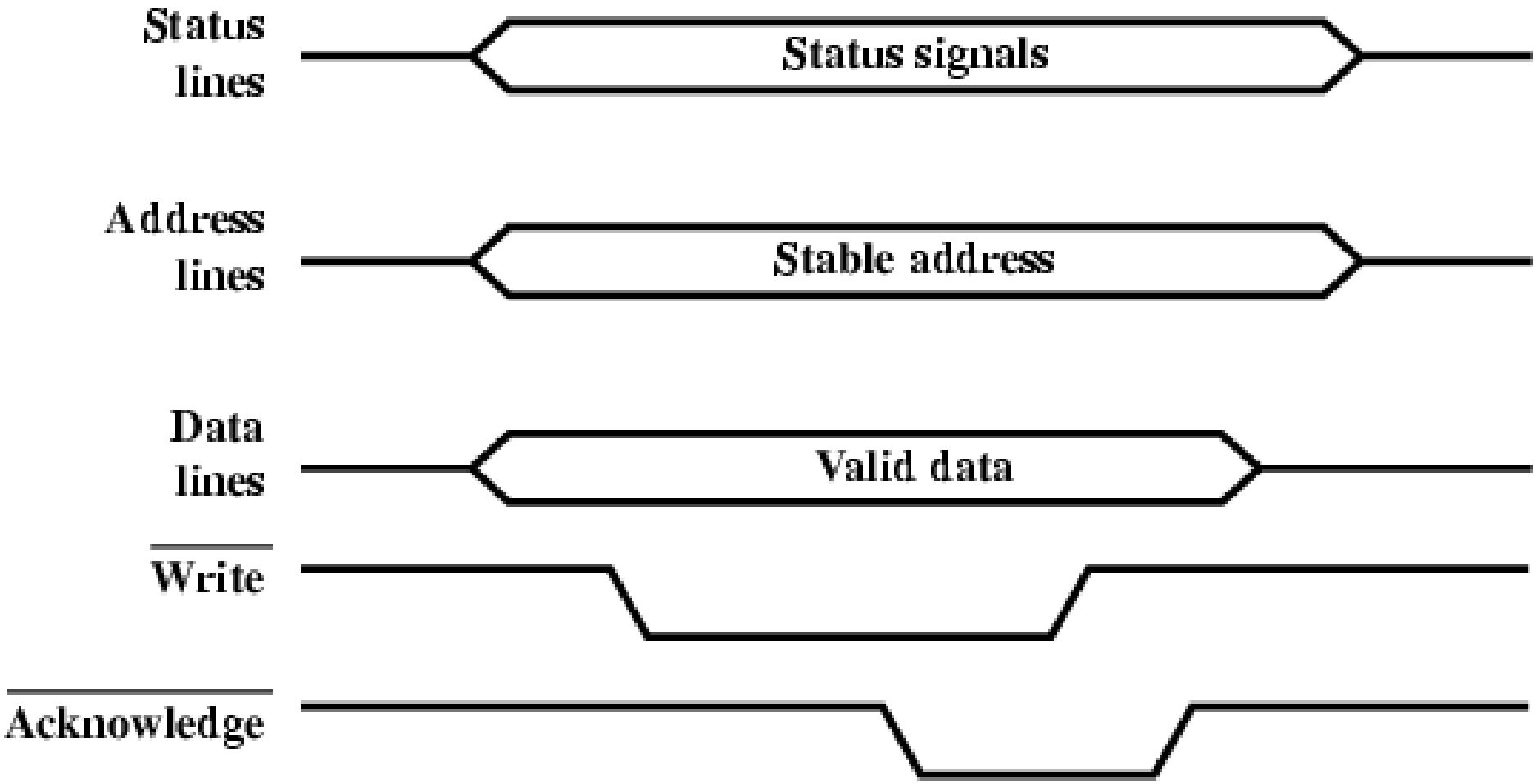
SYNCHRONOUS TIMING DIAGRAM



ASYNCHRONOUS TIMING – READ DIAGRAM



ASYNCHRONOUS TIMING – WRITE DIAGRAM



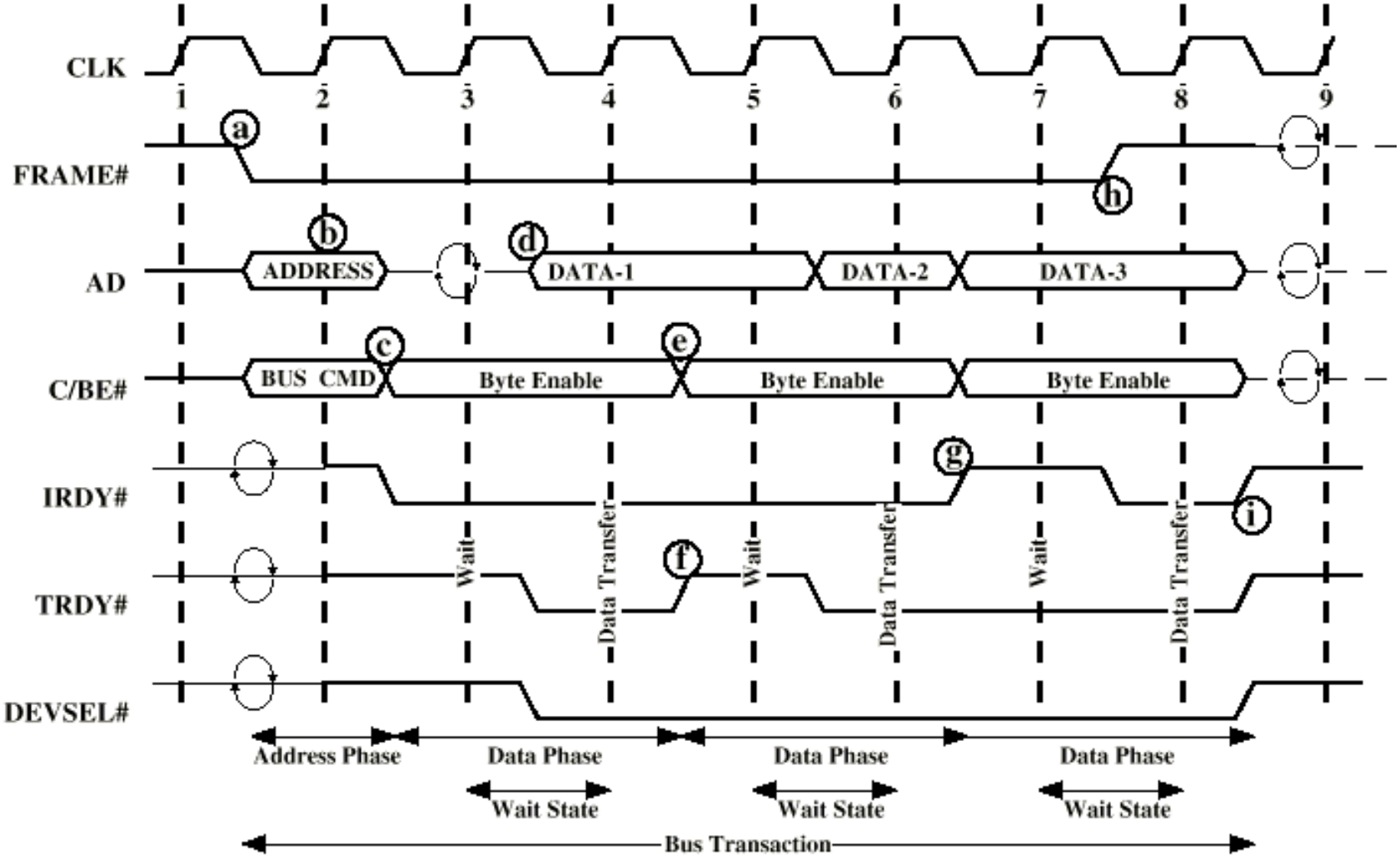
PCI BUS

- Peripheral Component Interconnection (PCI)
- Intel released to public domain
- 32 or 64 bit
- 50 lines
- Systems lines
  - Including clock and reset
- Address & Data
  - 32 time mux lines for address/data
  - Interrupt & validate lines
- Interface Control
- Arbitration
  - Not shared
  - Direct connection to PCI bus arbiter
- Error lines

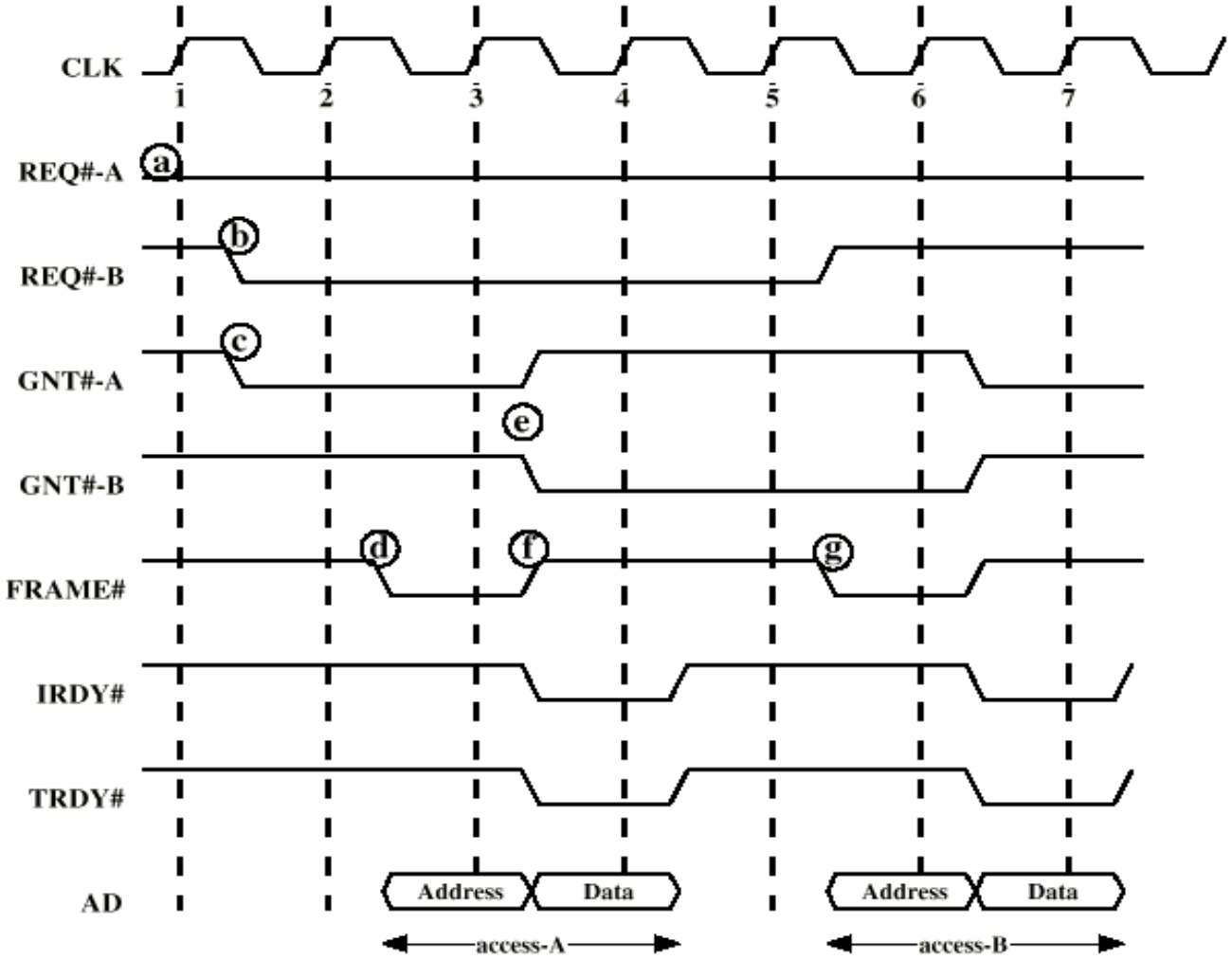
PCI COMMANDS

- Transaction between initiator (master) and target
- Master claims bus
- Determine type of transaction
  - e.g. I/O read/write
- Address phase
- One or more data phases

PCI READ TIMING DIAGRAM



PCI BUS ARBITRATION



Multiple Choice Question

MUTIPLE CHOICE QUESTIONS:

Sr no	Question	Option A	Option B	OptionC	OptionD
1	The processor keeps track of the results of its operations using flags called _____	Test output flags	Conditional code flag	Type flags	None of the mentioned
2	The register used to store the flags is called as _____	Flag Register	Status register	Test register	Log register
3	The Flag 'V' is set to 1 indicates that _____	The operation is valid	The operation is validated	The operation has resulted in an overflow	None of the mentioned
4	In some pipelined systems, a different instruction is used to add to numbers which can affect the flags upon execution. That instruction is _____	AddSetCC	AddCC	Add++	SumSetCC
5	The most efficient method followed by computers to multiply two unsigned numbers is _____	Booth algorithm	Bit pair recording of multipliers	Restoring algorithm	Non restoring algorithm

REFERENCES

- http://www.engppt.com/search/label/Computer%20Organization%20and%20Architecture
- http://www.engppt.com/search/label/Computer%20Architecture%20ppt