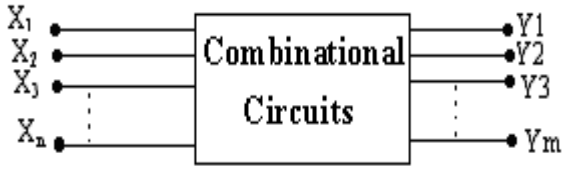
FACULTY OF ENGINEERING & TECHNOLOGY

Combinational Circuits

The combinational circuits are the network of logic gates having a set of input independent variables, and outputs as the Boolean functions inputs. The output variables in these circuits depend only on the present value of the inputs and do not depend upon their previous values.

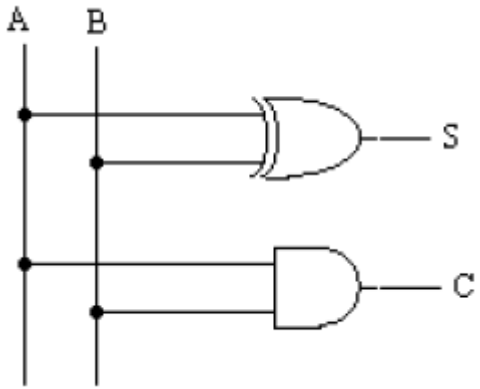


Half Adder

A half adder is combinational circuits which adds two binary digits simultaneously

Circuit Diagram
Truth Table

Inputs		Outputs	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	1	1



Symbolic representation of the half adder

Sum S and Carry C are given by

$$S = \overline{A} \cdot B + A \cdot \overline{B}$$
$$= A \oplus B$$
$$C = A \cdot B$$

Q1: Design the half adder using NOR gates only.

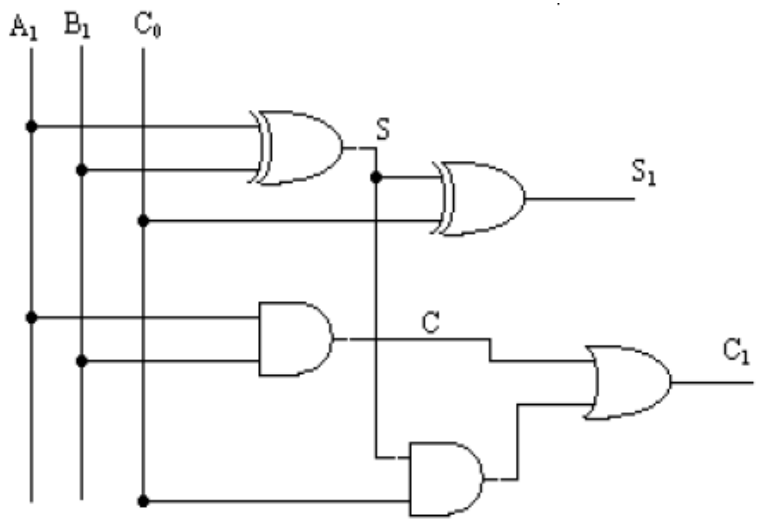
Full Adder

A Full adder is combinational circuits which adds three binary digits simultaneously

Circuit Diagram

Truth Table

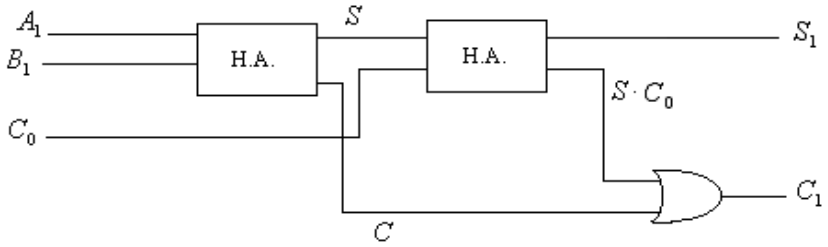
A_1	B_1	C_0	S_1	C_1
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



Sum S1 & Carry C_1 are given by

$$S_1=A_1 \oplus B_1 \oplus C_0$$
$$C_1= (A_1 \oplus B_1)C_0+A_1B_1$$

It is clear that a full adder consists of two half adders and an OR gate



Multiplexers

A multiplexer (MUX) also known as data selector, is a logic circuit which allows the digital information from multi-inputs to a single output line. The selection of the input data to be routed to the output line is done by the select terminals. The number of select terminals depends on the number of input lines to be routed to output line, given by the general formula as:

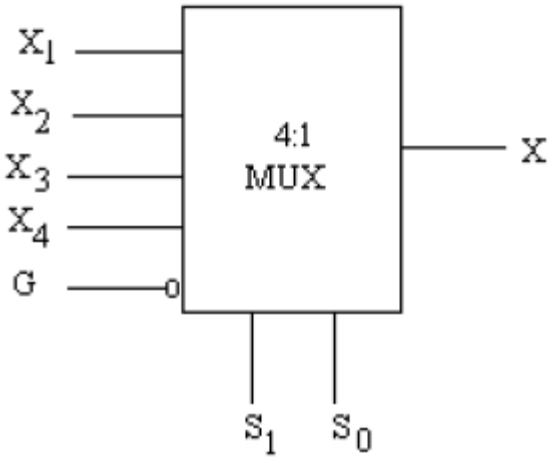
$$2^K=N$$

where N is the number of input lines
K is the number of select terminals.

Example. if there are 4 input lines to be routed to output line, then two select terminals are needed as $2^2=4$.

The output X will follow the input data depending on the select terminals S_1,S_0 ,as given in the table

Select terminals		Output
S_1	S_0	X
0	0	$X=X_0$
0	1	$X=X_1$
1	0	$X=X_2$
1	1	$X=X_3$

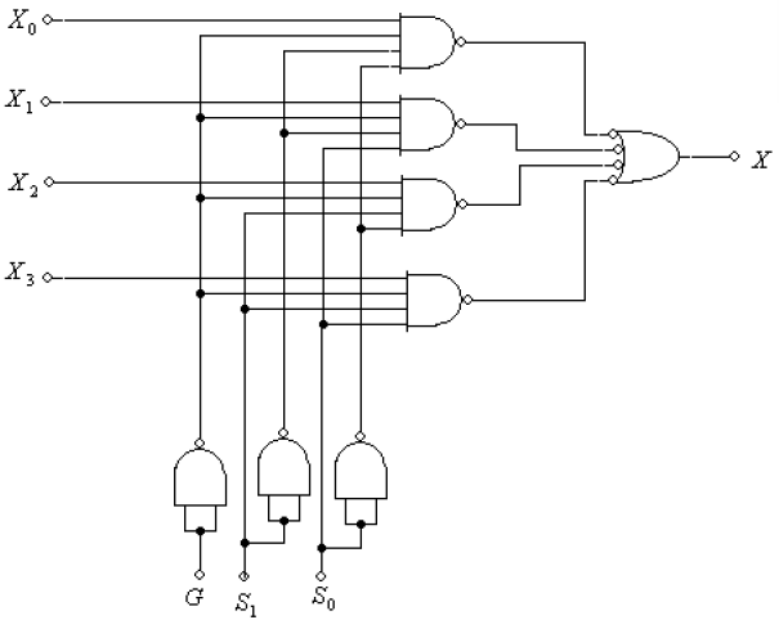


The block diagram for 4:1 multiplexer

COMBINATIONAL CIRCUITS

The Boolean function to perform the multiplexing action is given as:

$$X = X_0 \cdot \overline{S}_1 \cdot \overline{S}_0 + X_1 \cdot \overline{S}_1 \cdot S_0 + X_2 \cdot S_1 \cdot \overline{S}_0 + X_3 \cdot S_1 \cdot S_0$$



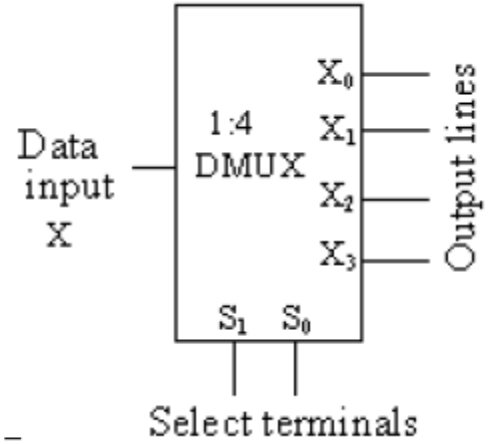
Q 2: Use Multiplexers to implement of Full adder

Demultiplexers

A demultiplexer performs the reverse process of multiplexer; it receives the information on a single line and steers to several output lines. Demultiplexer can also be called the Data Distributor as it can transmit the same data to the different lines. It transmits the data to 2^N output lines, for which the select terminals of N bits are required.

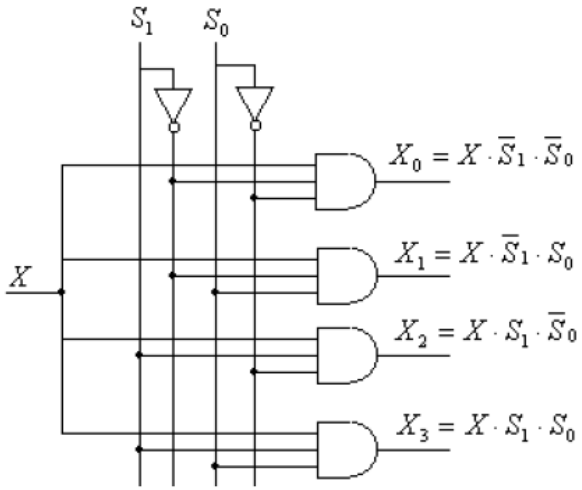
Example. To transmit the single data to four output lines (1:4 DMUX), select terminals of two bits are required

If S_1,S_0 = 00 , the input data X will be go to the output X_0
If S_1,S_0 = 01 , the input data X will be go to the output X_1
If S_1,S_0 = 10 , the input data X will be go to the output X_2
If S_1,S_0 = 11 , the input data X will be go to the output X_3



The Boolean expressions for X0, X1, X2, X3 are given by:

$$X_0 = X \cdot \overline{S}_1 \cdot \overline{S}_0$$
$$X_1 = X \cdot \overline{S}_1 \cdot S_0$$
$$X_2 = X \cdot S_1 \cdot \overline{S}_0$$
$$X_3 = X \cdot S_1 \cdot S_0$$



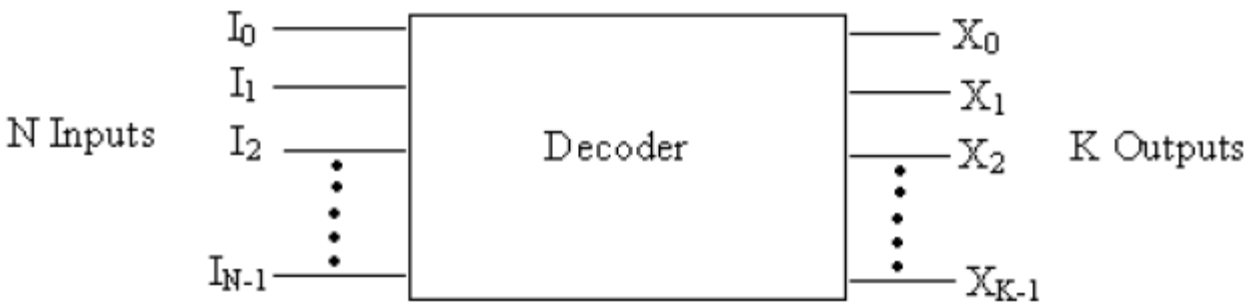
Decoder

A decoder is a logic circuit which has a set of inputs representing a binary number and gives only one output corresponding to the input number. The decoder activates one output at a time depending upon the input binary number; all other outputs will be inactive.

The possible combinations of N inputs will be

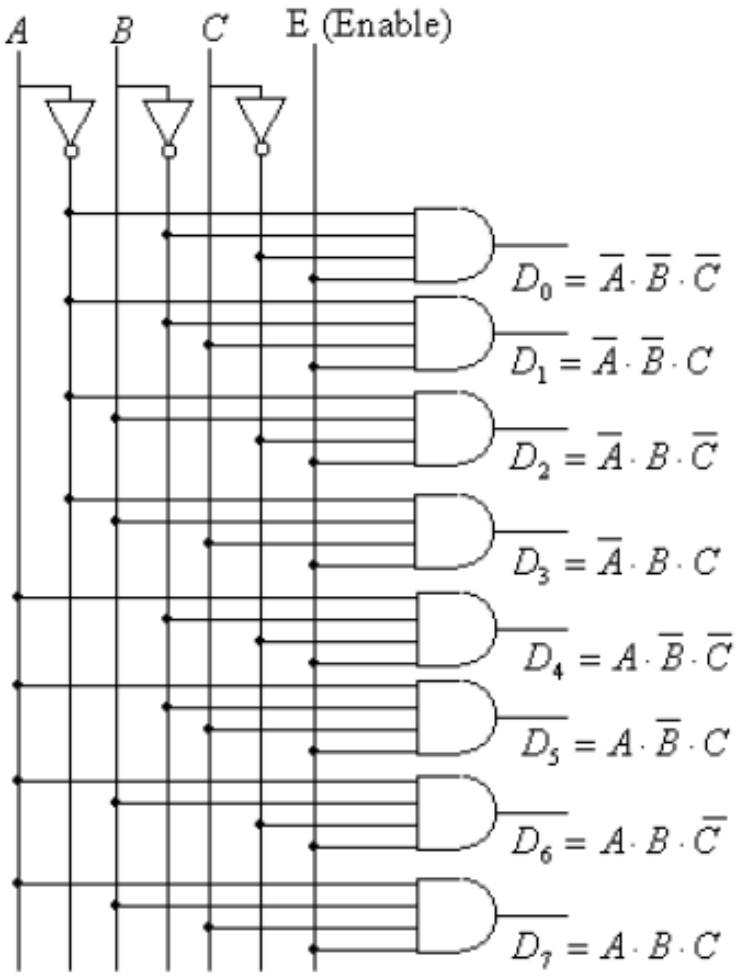
$$2^N=K$$

Where K will be outputs.



Block Diagram of a decoder having N inputs and K outputs

Circuit diagram of 3 – to – 8 line decoder

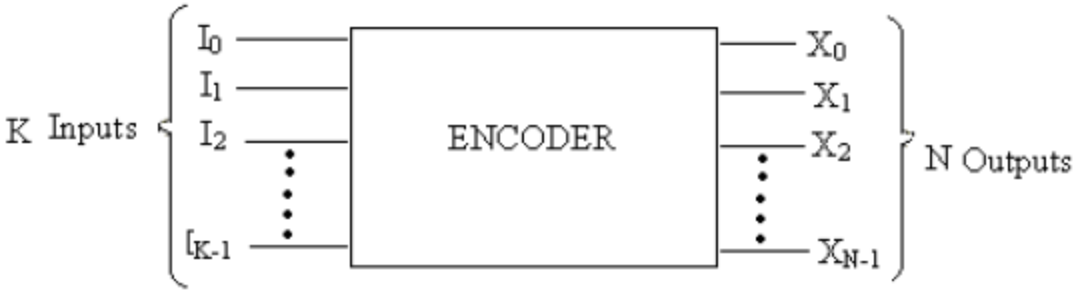


Truth Table of 3 – to – 8 line decoder

Inputs			Enable	Outputs							
A	B	C	E	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
ø	ø	ø	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0	1
0	0	1	1	0	0	0	0	0	0	1	0
0	1	0	1	0	0	0	0	0	1	0	0
0	1	1	1	0	0	0	0	1	0	0	0
1	0	0	1	0	0	0	1	0	0	0	0
1	0	1	1	0	0	1	0	0	0	0	0
1	1	0	1	0	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0

Encoders

An encoder a combinational circuit which performs the reverse operation of decoder. The decoder accepts N bit input code and activates one of the several out lines corresponding to that code. However, an encoder has a number of input lines, only one of which is activated at a time. It provides the N bit code at the output corresponding to activated input line. The decoders studied in the foregoing section were binary to octal, BCD to decimal decoder etc. The encoders will therefore, be like octal to binary and decimal to BCD encoders. In the K input lines only one line will be high at a time.



Block Diagram of an encoder having K inputs and N outputs

BCD – to – Seven – Segment Decoder

A decoder for BCD to 7 – segment will now be discussed. A seven segment display consists of seven display lights (segments) arranged in a pattern shown in figure. The light emitting gallium arsenide or phosphide diodes are generally used for the segments of these display devices. These devices, also known as seven – segment LED display devices, are operated at low voltage and low power and hence directly connected to ICs. The segments of the display devices are marked as a, b, c, d, e, f, g. The numeric digits 0 through 9 may be displayed if the corresponding segments glow as shown in figure 6.20 by the darken segments.

The seven – segment LED display devices are of two types, one is known as common cathode and the other is known as common anode. In the common cathode LED display device, the cathodes of all its LEDs are connected to the common terminal of the device. When the common terminal is grounded and positive voltages are applied to the anodes of the corresponding LEDs of the display device, then the numerals will be displayed on the devices. However, in the common anode LED display devices, the anodes of all its LEDs are connected to the common terminal of the device which is to be connected to the positive supply; and when the low voltages are applied to the anodes of the devices, the numerals are displayed. BCD to seven - segment decoders are available in the form of ICs. The common cathode LED display devices are connected to such BCD to seven segment decoder ICs which provide active high outputs and common anode LED display devices to such decoder ICs which provide active low outputs. Other display devices are LCD (Liquid Crystal Devices). The design of a combinational circuit will be discussed. It will decode 4 – bit BCD codes to decimal digits. The logic circuit will have 4 inputs and seven outputs as shown in figure. Seven outputs will correspond to the segments of the display.