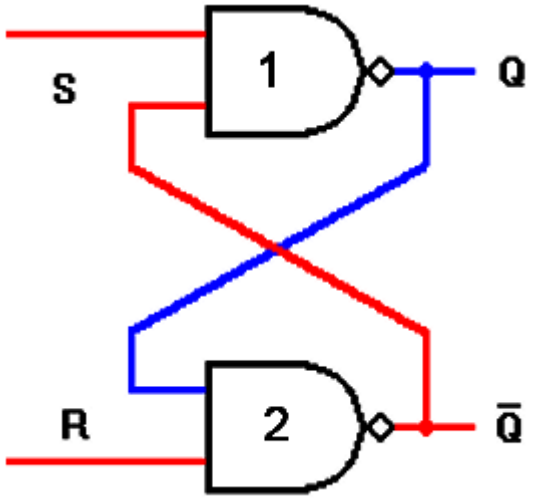
FACULTY OF ENGINEERING & TECHNOLOGY

Dileep Kumar
Assistant Prof. EE Deptt

FLIP-FLOP

a.SR Flip Flop Active Low = NAND gates [SR Flip Flop - NAND GATE LATCH]

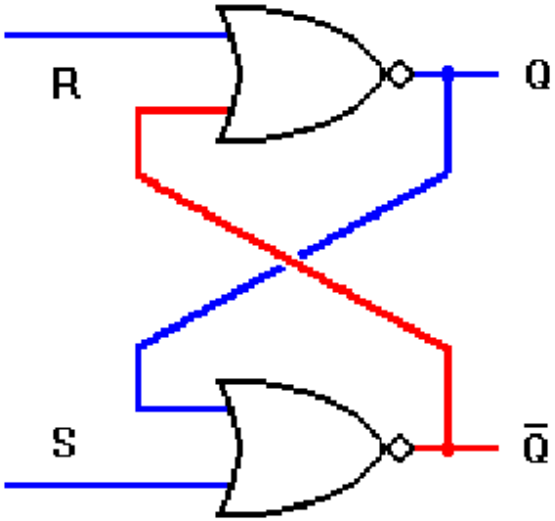


- The NAND gate version has two inputs, SET (S) and RESET (R).
- Two outputs, Q as normal output and $\bar{Q}$ as inverted output and feedback mechanism.
- The feedback mechanism is required to form a sequential circuit by connecting the output of NAND-1 to the input of NAND-2 and vice versa.
- The circuit outputs depends on the inputs and also on the outputs.

- From the description of the NAND gate latch operation, it shows that the SET and RESET inputs are active LOW.
- The SET input will set Q = 1 when SET is 0 (LOW).RESET input will reset Q = 0 when RESET is 0 (LOW)
- In the prohibited/INVALID state both outputs are 1. This condition is not used on the RS flip-flop. The set condition means setting the output Q to 1.
- Likewise, the reset condition means resetting (clearing) the output Q to 0. The last row shows the disabled, or hold , condition of the RS flip-flop. The outputs remain as they were before the hold condition existed. There is no change in the outputs from the previous states

S	R	Q	$\bar{Q}$	STATUS
0	0	1	1	**INVALID**
0	1	1	0	**SET**
1	0	0	1	**RESET**
1	1	Q	$\bar{Q}$	**HOLD** (NoChange)

b. SR Flip Flop Active High = NOR gates [SR Flip Flop - NOR GATE]



S	R	Q	$\bar{Q}$	STATUS
0	0	Q	$\bar{Q}$	HOLD (NoChange)
0	1	0	1	RESET
1	0	1	0	SET
1	1	0	0	INVALID

- The latch circuit can also be constructed using two NOR gates latch.
- The construction is similar to the NAND latch except that the normal output Q and inverted output $\bar{Q}$ have reversed positions.
- S = 1, R = 0; This will set Q to 1, it works in SET mode operation.
- S = 1, R = 1; This condition tries to set and reset the NOR gate latch at the same time, and it produces Q = $\bar{Q}$ = 0 This is an unexpected condition and are not used.
- Since the two outputs should be inverse of each other. If the inputs are returned to 1 simultaneously, the output states are unpredictable.
- This input condition should not be used and when circuits are constructed, the design should make this condition SET=RESET = 1 never arises.
- From the description of the NOR gate latch operation, it shows that the SET and RESET inputs are Active HIGH.
- The SET input will set Q = 1 when SET is 1 (HIGH). RESET input will reset Q when RESET is 1 (HIGH).

The CLOCK

- When the clock changes from a LOW state to a HIGH state, this is called the positive-going transition (PGT) or positive edge triggered.
- When the clock changes from a HIGH state to a LOW state, it is called negative going transition (NGT) or negative edge triggered.