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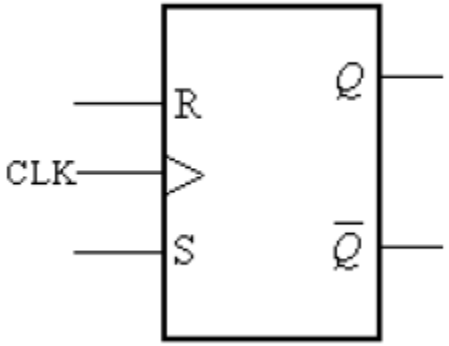
Clocked SR Flip Flop

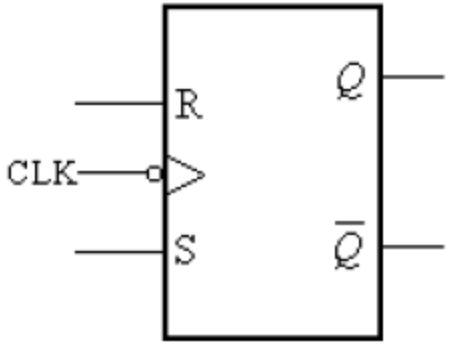
- Additional clock input is added to change the SR flip- flop from an element used in asynchronous sequential circuits to one, which can be used in synchronous circuits.
- The clocked SR flip flop logic symbol that is triggered by the PGT is shown in Figure.
- Its means that the flip flop can change the output states only when clock signal makes a transition from LOW to HIGH.
- The Truth Table in figure shows how the flip flop output will respond to the PGT at the clocked input for the various combinations of SR inputs and output.
- The up arrow symbol indicates PGT.
- The clocked SR Flip Flop logic symbol that is triggered by the NGT is shown in Figure.
- It means that the Flip flop can change the output states only when clocked signal makes a transition from HIGH to LOW

PGT Clocked SR Flip Flop Symbol



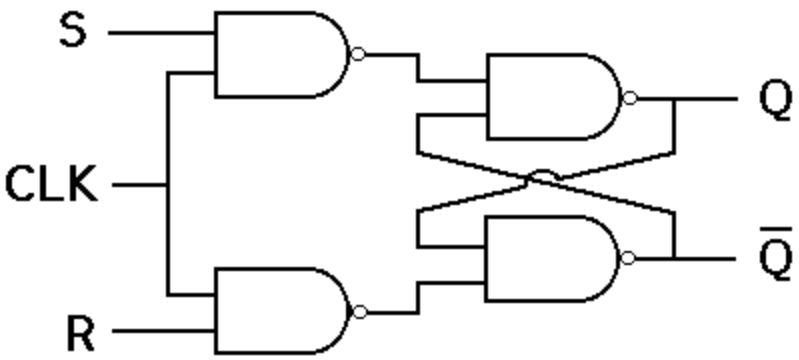
clock	S	R	Q	$\overline{Q}$	STATUS
↑	0	0	Q	$\overline{Q}$	HOLD (NoChange)
↑	0	1	0	1	RESET
↑	1	0	1	0	SET
↑	1	1	0	0	INVALID

NGT Clocked SR Flip Flop Symbol

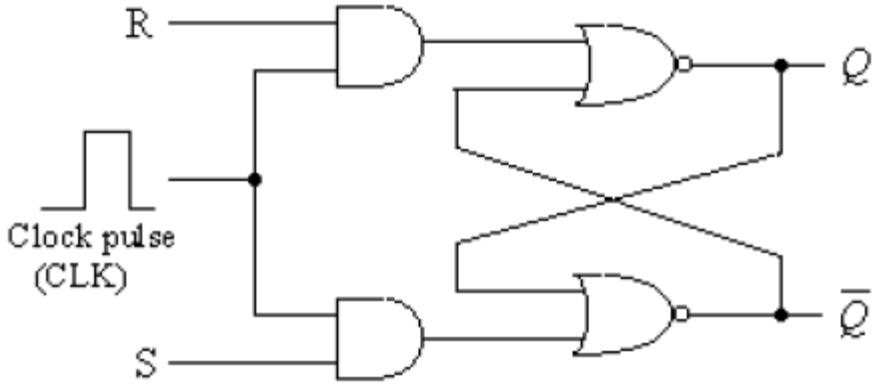


Clocked SR Flip Flop Logic Circuit

If used NAND Gate

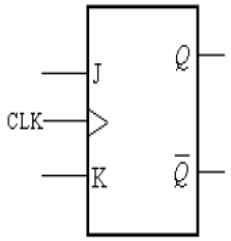


If used NOR Gate , must used AND Gate in front.

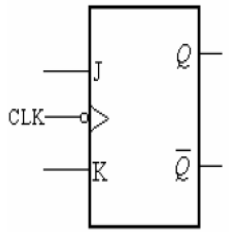


JK Flip Flop - Symbol & Truth Table

- Another types of Flip flop is JK flip flop.
- It differs from the RS flip flops when J=K=1 condition is not indeterminate but it is defined to give a very useful changeover (toggle) action.
- Toggle means that Q and $\overline{Q}$ will switch to their opposite states.
- The JK Flip flop has clock input Cp and two control inputs J and K.
- Operation of JK Flip Flop is completely described by truth table in Figure.



J_n	K_n	Q_n	Clock	Q_{n+1}	
0	0	0	↑	0	No Change
0	0	1	↑	1	
0	1	0	↑	0	Reset
0	1	1	↑	0	
1	0	0	↑	1	Set
1	0	1	↑	1	
1	1	0	↑	1	Complement
1	1	1	↑	0	



J_n	K_n	Q_n	Clock	Q_{n+1}	
0	0	0	↓	0	No Change
0	0	1	↓	1	
0	1	0	↓	0	Reset
0	1	1	↓	0	
1	0	0	↓	1	Set
1	0	1	↓	1	
1	1	0	↓	1	Complement
1	1	1	↓	0	

JK Flip Flop –Logic Circuit