RAMA UNIVERSITY

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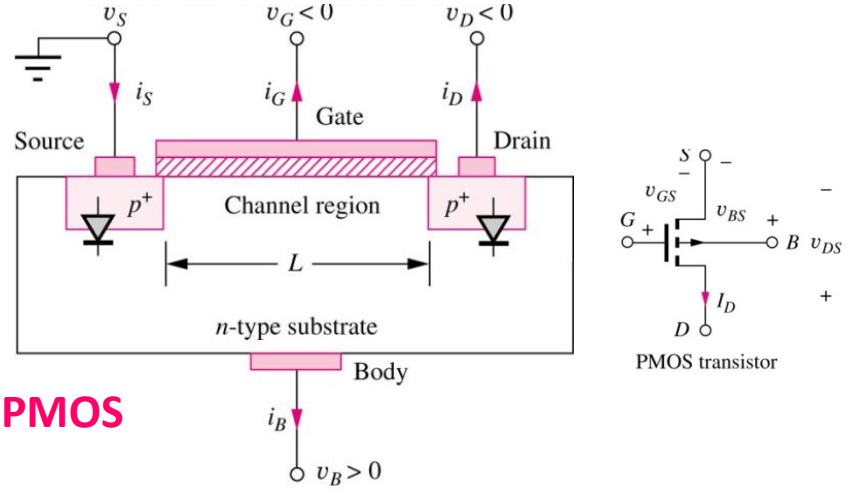
FACULTY OF ENGINEERING AND TECHNOLOGY

MEC-022

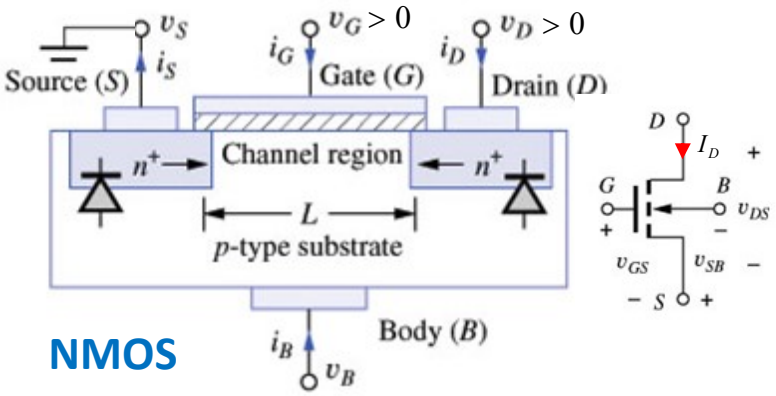
Lecture - 10

PMOS Transistors Structure (Enhancement-Mode)



PMOS

- *P*-type source and drain regions in *n*-type substrate.
- $v_{GS} < 0$ required to create p-type inversion layer in channel region



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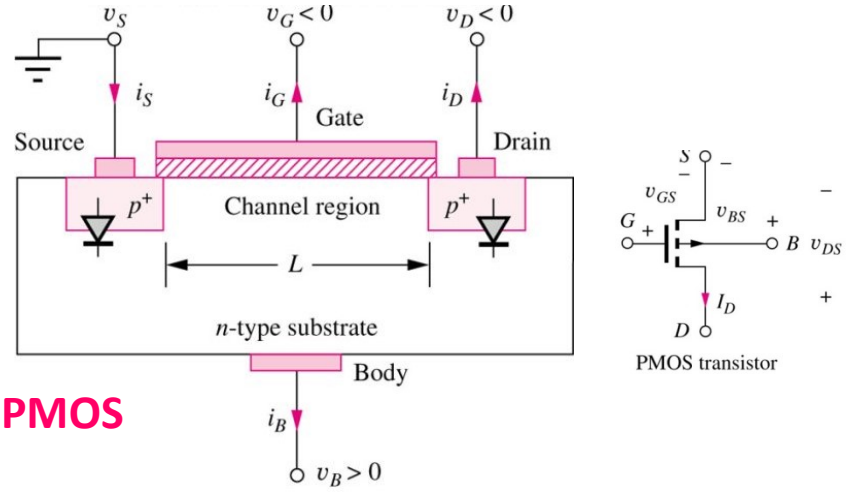

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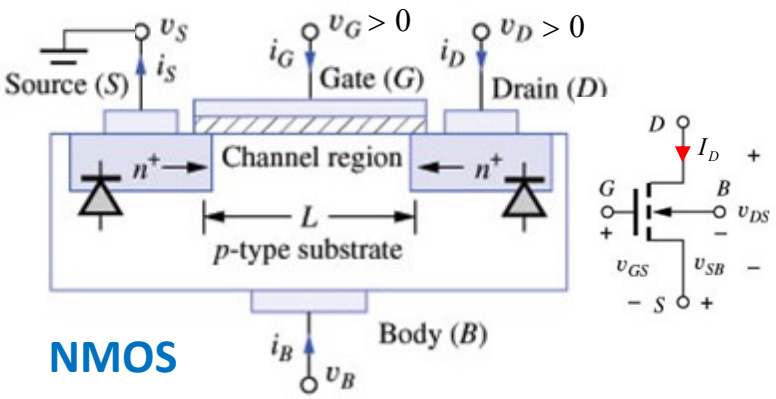

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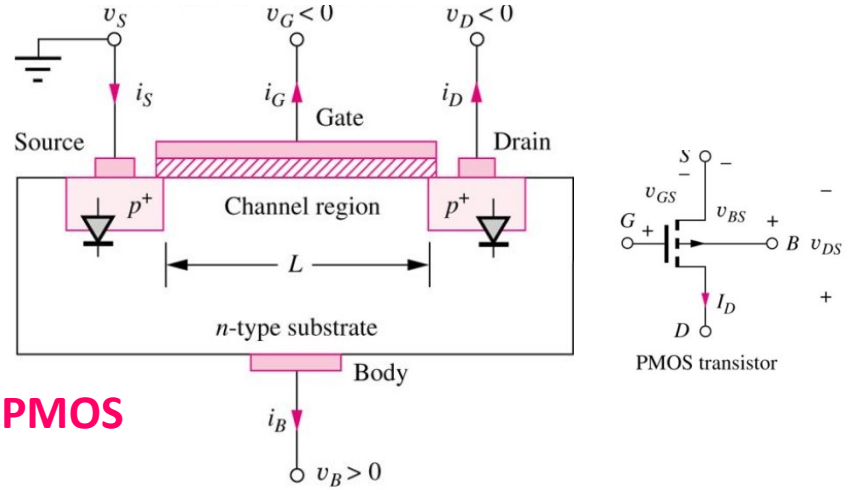

PMOS

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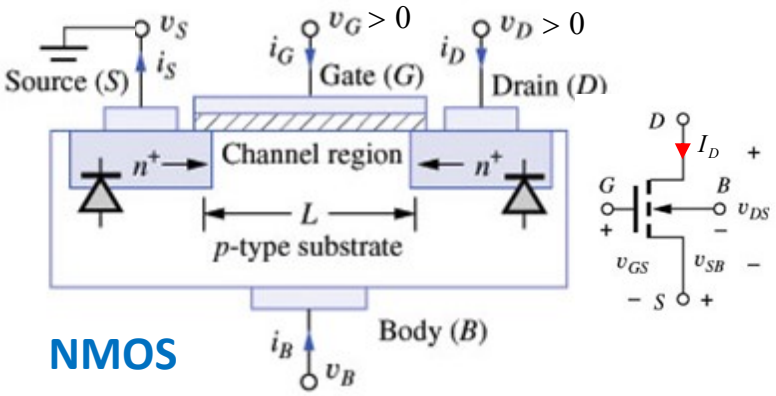
- To maintain reverse bias on diodes of source-substrate and drain-substrate junctions:
  $v_{SB} < 0$ and $v_{DB} < 0$



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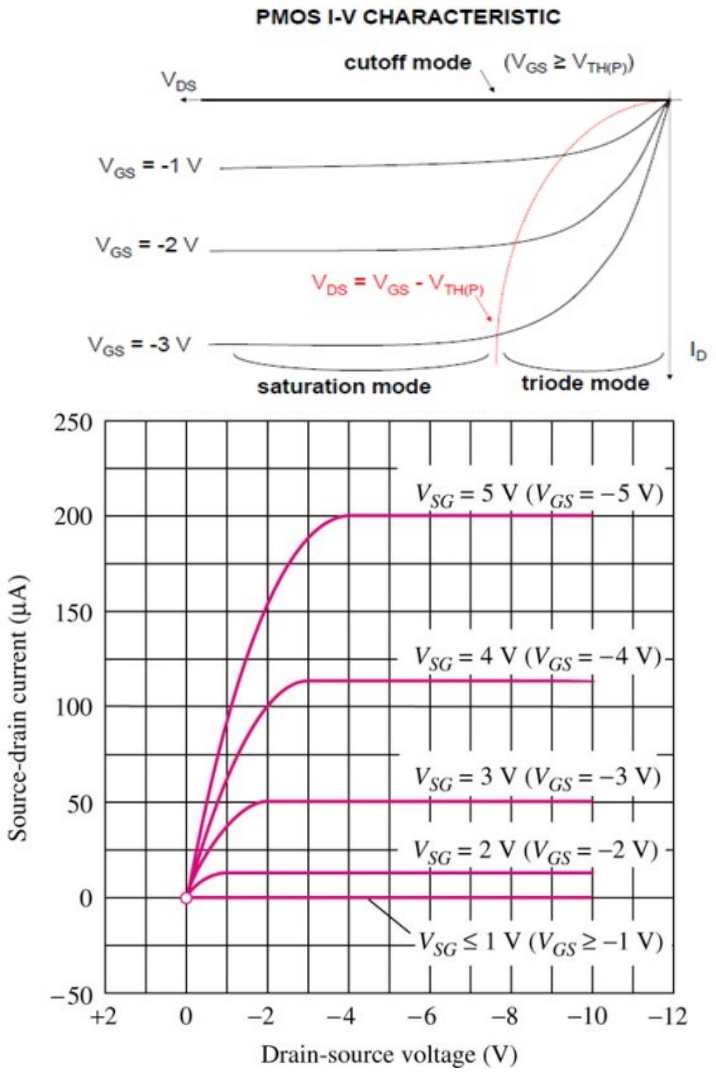
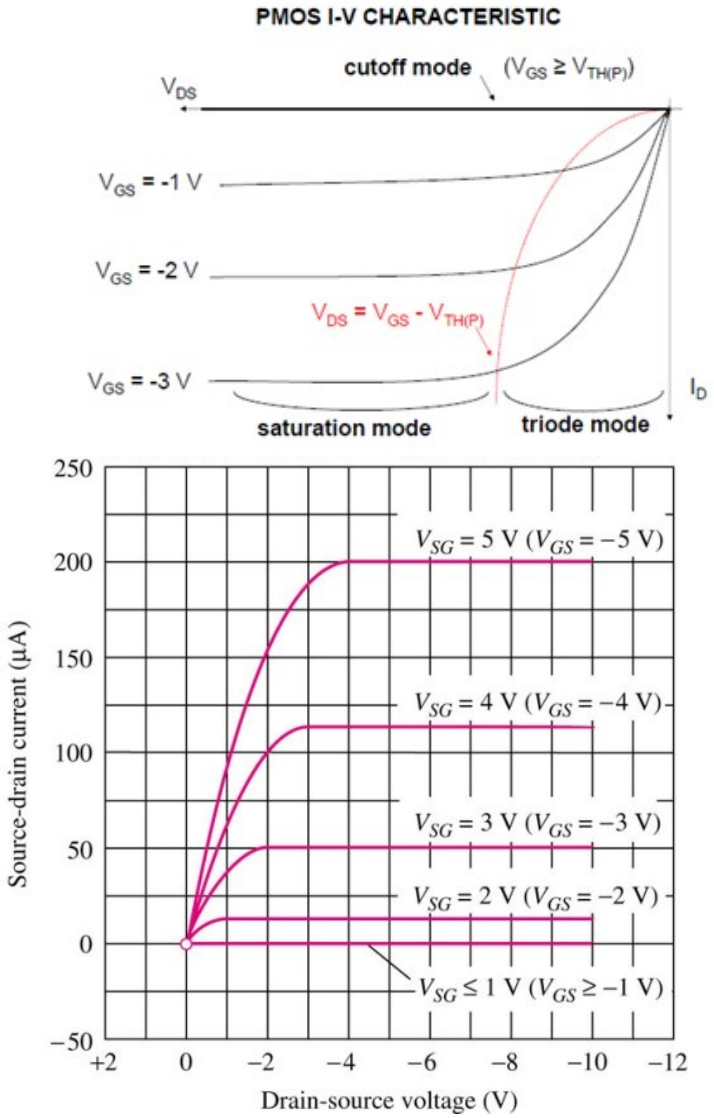
Enhancement-Mode PMOS Transistors: Output Characteristics



- For the PMOS transistor, all parameters and behavior are inverse of NMOS transistor.
- Thus the output characteristics of PMOS are the complete inverse of those of NMOS
- Often, they are shown in the inverted scale and then they look very similar to the characteristics of NMOS

Enhancement-Mode PMOS Transistors: Output Characteristics



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- For $V_{GS} \geq V_{TP}$ transistor is off (note that on the diagram it's $v_{SG} = - v_{GS}$).

NMOS Summary (model)

For all regions,

$$K_n = K_n' \frac{W}{L} \qquad K_n' = \mu_n C_{\text{ox}}'' \qquad i_G = 0 \qquad i_B = 0 \tag{4.24}$$

Cutoff region:

$$i_D = 0 \qquad \text{for } v_{GS} \leq V_{TN} \tag{4.25}$$

Triode region:

$$i_D = K_n \left(v_{GS} - V_{TN} - \frac{v_{DS}}{2} \right) v_{DS} \qquad \text{for } v_{GS} - V_{TN} \geq v_{DS} \geq 0 \tag{4.26}$$

Saturation region:

$$i_D = \frac{K_n}{2} (v_{GS} - V_{TN})^2 (1 + \lambda v_{DS}) \qquad \text{for } v_{DS} \geq (v_{GS} - V_{TN}) \geq 0 \tag{4.27}$$

Threshold voltage:

$$V_{TN} = V_{TO} + \gamma \left(\sqrt{v_{SB} + 2\phi_F} - \sqrt{2\phi_F} \right) \tag{4.28}$$

For the enhancement-mode NMOS transistor, $V_{TN} > 0$. For the depletion-mode NMOS, $V_{TN} < 0$.


Thank You!