RAMA UNIVERSITY

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FACULTY OF ENGINEERING AND TECHNOLOGY

MEC-022

Lecture - 11

PMOS Summary (model)

For all regions,

$$K_p = K'_p \frac{W}{L} \qquad K'_p = \mu_p C''_{ox} \qquad i_G = 0 \qquad i_B = 0 \tag{4.29}$$

Cutoff region:

$$i_D = 0 \qquad \text{for } V_{GS} \geq V_{TP} \tag{4.30}$$

Triode region:

$$i_D = K_p \left(v_{GS} - V_{TP} - \frac{v_{DS}}{2} \right) v_{DS} \qquad \text{for } 0 \leq |v_{DS}| \leq |v_{GS} - V_{TP}| \tag{4.31}$$

Saturation region:

$$i_D = \frac{K_p}{2} (v_{GS} - V_{TP})^2 (1 + \lambda |v_{DS}|) \qquad \text{for } |v_{DS}| \geq |v_{GS} - V_{TP}| \geq 0 \tag{4.32}$$

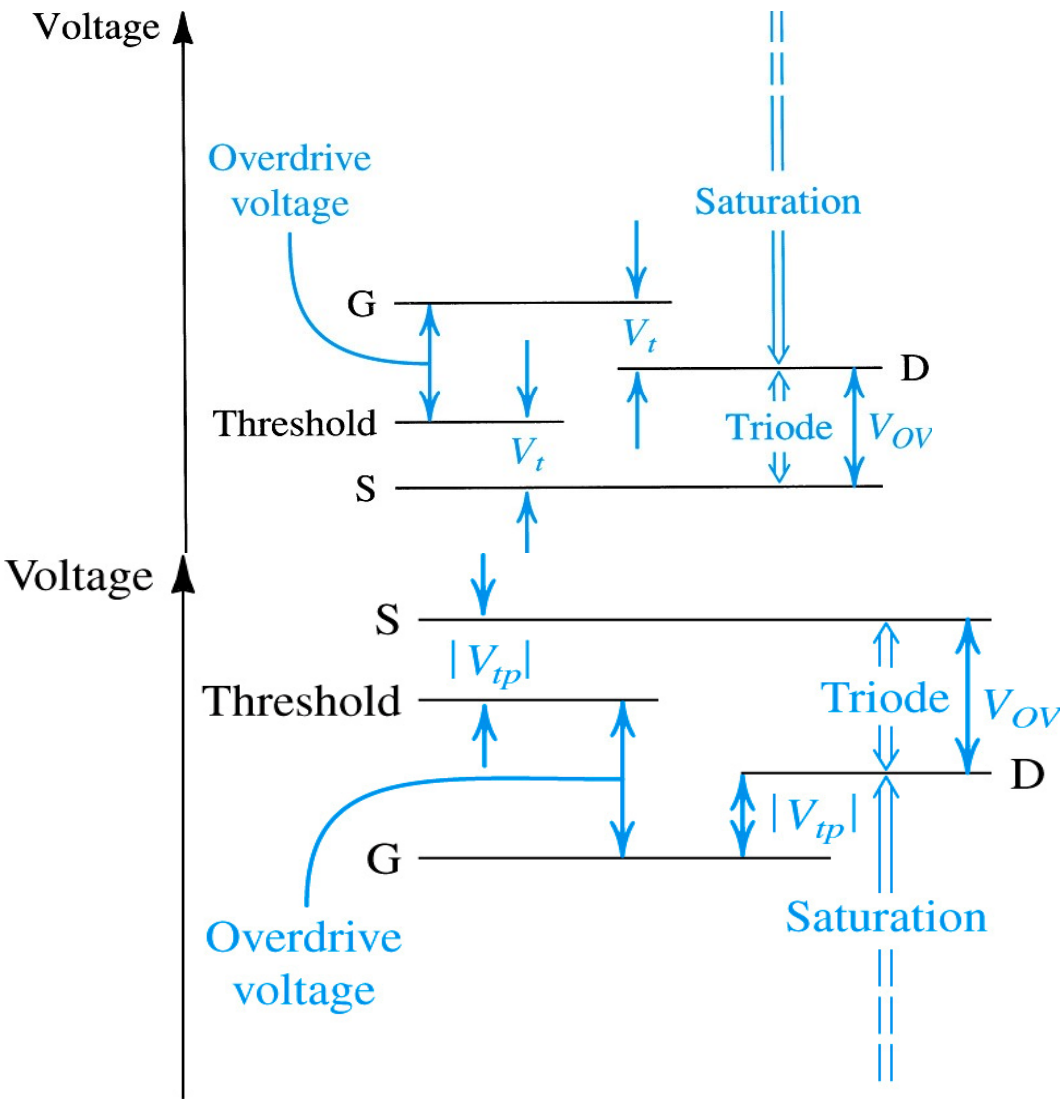
Threshold voltage:

$$V_{TP} = V_{TO} - \gamma \left(\sqrt{v_{BS} + 2\phi_F} - \sqrt{2\phi_F} \right) \tag{4.33}$$

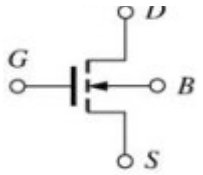
be

For the enhancement-mode PMOS transistor, $V_{TP} < 0$. For the depletion-mode PMOS, $V_{TP} > 0$.

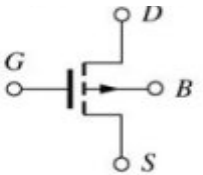
NMOS and PMOS Summary (terminal voltages)



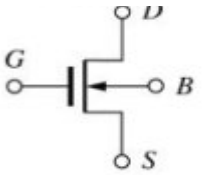
MOSFET Circuit Symbols



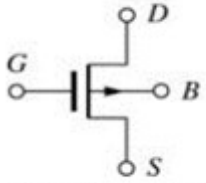
(a) NMOS enhancement-mode device



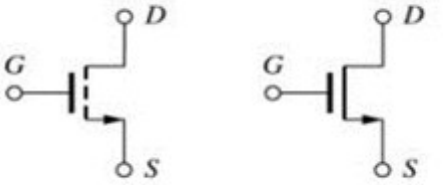
(b) PMOS enhancement-mode device



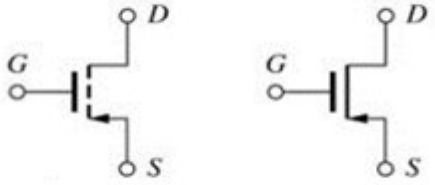
(c) NMOS depletion-mode device



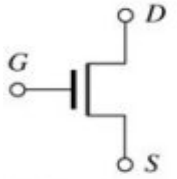
(d) PMOS depletion-mode device



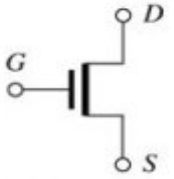
(e) Three-terminal NMOS transistors



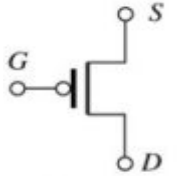
(f) Three-terminal PMOS transistors



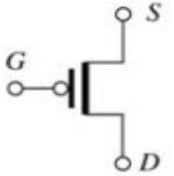
(g) Shorthand notation—NMOS enhancement-mode device



(h) Shorthand notation—NMOS depletion-mode device



(i) Shorthand notation—PMOS enhancement-mode device

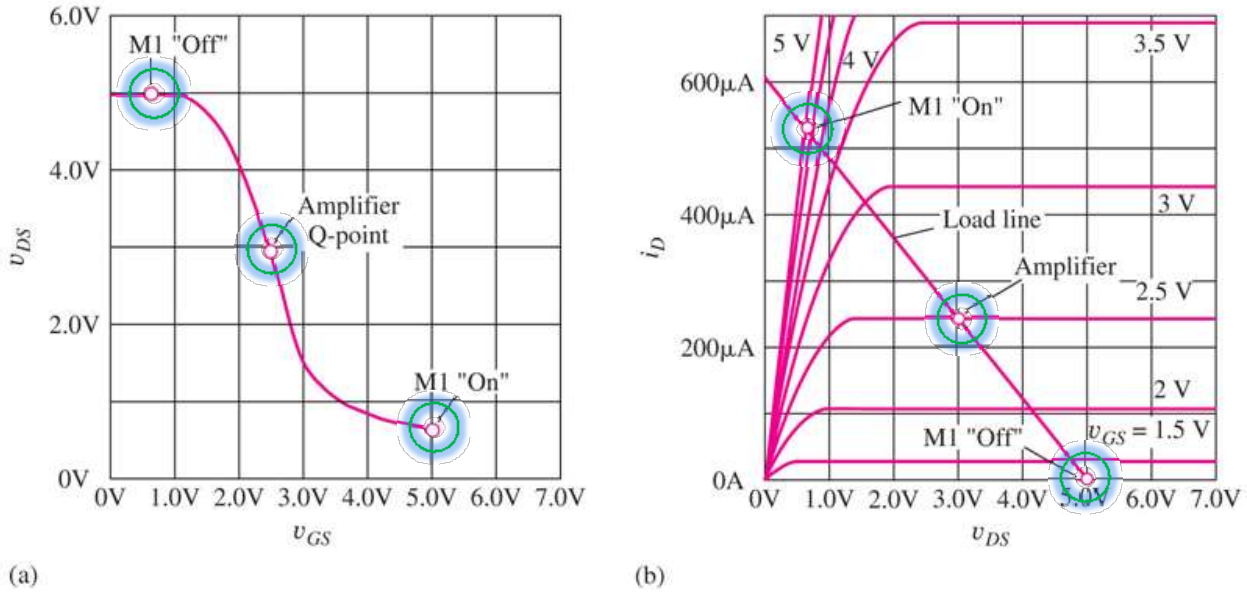


(j) Shorthand notation—PMOS depletion-mode device

- (g) and (i) are the most commonly used symbols in VLSI logic design.
- MOS devices are symmetric.
- In NMOS, n^+ region at higher voltage is the drain.
- In PMOS p^+ region at lower voltage is the drain

MOSFET Analysis

- Depending on the type of application, a MOSFET may be put into one of three regions of operation by setting its operating **Q-point** .




Thank You!