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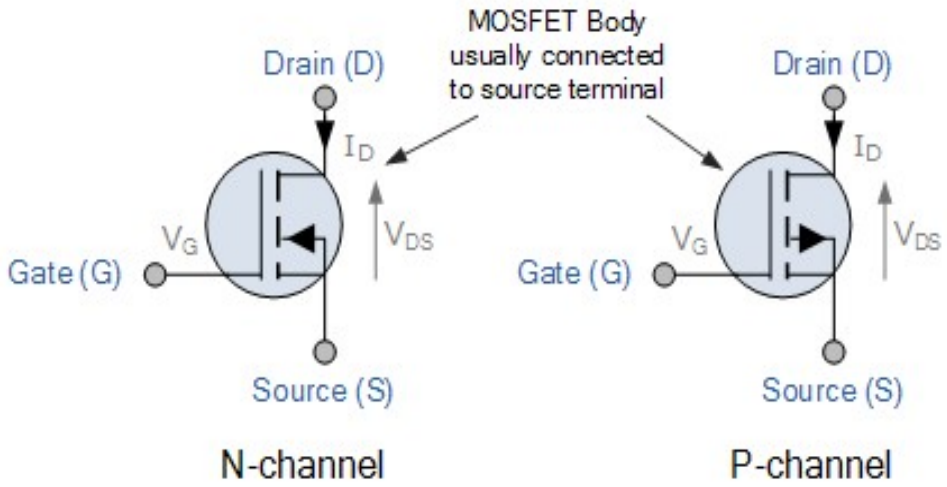
# FACULTY OF ENGINEERING AND TECHNOLOGY

## MEC-022

## Lecture - 02

The reverse is true for the p-channel enhancement MOS transistor. When $V_{GS}$ = 0 the device is “OFF” and the channel is open. The application of a negative (-ve) gate voltage to the p-type eMOSFET enhances the channels conductivity turning it “ON”. Then for an p-channel enhancement mode MOSFET: $+V_{GS}$ turns the transistor “OFF”, while $-V_{GS}$ turns the transistor “ON”.

Enhancement-mode MOSFETs make excellent electronics switches due to their low “ON” resistance and extremely high “OFF” resistance as well as their infinitely high input resistance due to their isolated gate. Enhancement-mode MOSFETs are used in integrated circuits to produce CMOS type *Logic Gates* and power switching circuits in the form of as PMOS (P-channel) and NMOS (N-channel) gates. CMOS actually stands for *Complementary MOS* meaning that the logic device has both PMOS and NMOS within its design.



# Two states enables it to have two basic

Switching(digital electronics)
Amplification (analogue electronics)

**1. Cut-off Region** – with $V_{GS} < V_{threshold}$ the gate-source voltage is much lower than the transistors threshold voltage so the MOSFET transistor is switched "fully-OFF" thus, $I_D = 0$, with the transistor acting like an open switch regardless of the value of $V_{DS}$.

**2. Linear (Ohmic) Region –** with $V_{GS} > V_{threshold}$ and $V_{DS} < V_{GS}$ the transistor is in its constant resistance region behaving as a voltage-controlled resistance whose resistive value is determined by the gate voltage, $V_{GS}$ level.

**3. Saturation Region –** with $V_{GS} > V_{threshold}$ and $V_{DS} > V_{GS}$ the transistor is in its constant current region and is therefore "fully-ON". The Drain current $I_D$ = Maximum with the transistor acting as a closed switch.

# Basic Electrical Properties of MOS

## THRESHOLD VOLTAGE

Since the drain and source are at the same voltage the channel carrier distribution is uniform along the device. The voltage at which the surface of the semiconductor gets inverted to the opposite polarity is known as Threshold voltage. In nMOS transistor, the surface will be inverted to n-type (remember in nMOS bulk is p-type silicon) and for pMOS transistor the surface will be inverted to p-type (remember in pMOS bulk is n-type silicon). At the threshold voltage condition, the concentration of electrons (holes) accumulated near the surface in a nMOS (pMOS) is equal to the doping concentration of the bulk doping concentration. Threshold voltage for nMOS is always positive and threshold voltage for pMOS is always negative.

An nMOS (pMOS) transistor has a conducting channel when the gate-source voltage is greater than (less than) threshold voltage, i.e., VGS > Vtn (VGS < Vtp).

$$V_{th} = V_{FB} + 2\phi_B + \frac{\sqrt{2qN_A \epsilon_{si} (2\phi_B + V_{SB})}}{C_{ox}} \qquad (2.1)$$

$V_{FB}$ = flat band voltage equal to $\phi_{ms}$
$\phi_{ms}$ = work function difference between gate and substrate
$N_A$ = substrate doping concentration
$\phi_B$ = energy difference between the Fermi level and intrinsic Fermi level in the semiconductor (silicon here) or Fermi voltage
$C_{ox}$ = oxide capacitance per unit area given by $\epsilon_{ox}/t_{ox}$ where $t_{ox}$ is the thickness of the oxide.

## THE SURFACE GETS INVERTED WHEN THE SURFACE POTENTIAL

Vth is a function of several components, most of which are material constants such as the difference in work function between gate and substrate material, the oxide thickness, the Fermi voltage. Apart from them the parameters shown below will also show their effect on the threshold voltage.

• If in the fabrication process some charges (sodium ions through human sweat, etc.) are trapped in the gate oxide, threshold voltage is altered as they show their reaction to the voltage applied to the gate. For example, if some positive ions are fixed in the oxide, the amount of positive charge required near the gate terminal to invert the surface decreases, hence threshold voltage decreases. If Qf is the charge in the oxide, the amount of extra voltage to be applied to the gate to neutralize these charges is given by – (Qf /Cox).

• Once the MOSFET is fabricated and if the threshold voltage has to be adjusted (increase or decrease) the only solution is to implant the dopants near the surface. This is known as threshold voltage adjustment implant and is given by VII = qDI/Cox. qDI is the charge implanted in the channel per unit area.

• TThe final expression with the above two effects included is given by

$$V_{th} = V_{FB} + 2\phi_B + \frac{\sqrt{2qN_A \in_{si} (2\phi_B + V_{SB})}}{C_{ox}} - \frac{Q_f}{C_{ox}} + \frac{qD_I}{C_{ox}}$$

## BODY EFFECT PARAMETER (Γ)

When VSB = 0 the threshold voltage reduces for the MOSFET reduces to that for the corresponding MOS capacitor. The effect of VSB on the threshold voltage can be expressed through the relation

$$\Delta V_{th} = V_{th} - V_{tho} = \gamma\left(\sqrt{2\phi_B + V_{SB}} - \sqrt{2\phi_B}\right)$$

# Field-Effect Transistors

- Describe structure and operation of MOSFETs.
- Define FET characteristics in operation regions of cutoff, triode and saturation.
- Develop mathematical models for *i*-*v* characteristics of MOSFETs.
- Introduce graphical representations for output and transfer characteristic descriptions of electron devices.
- Define and contrast characteristics of enhancement-mode and depletion-mode FETs.
- Define symbols to represent FETs in circuit schematics.
- Investigate circuits that bias transistors into different operating regions.
- Explore FET modeling in SPICE.
- Solid state transistor is the main building block of microelectronics.
- It performs two major functions used in electronic devices:
  - amplifications (in analog)
  - switching (in digital)
- There are two basic types of solid state transistors:
  BJT (bipolar junction transistor)
  FET (field effect transistor).

- FET: electric field is used to control the shape and the conductivity of the channel of **one type** charge carrier (*p* or *n*) in semiconductor device.
- They are also called unipolar to contrast their single-carrier-type operation with the **dual-carrier-type** operation of bipolar (junction) transistors (BJT).


Thank You!