
RAMA UNIVERSITY

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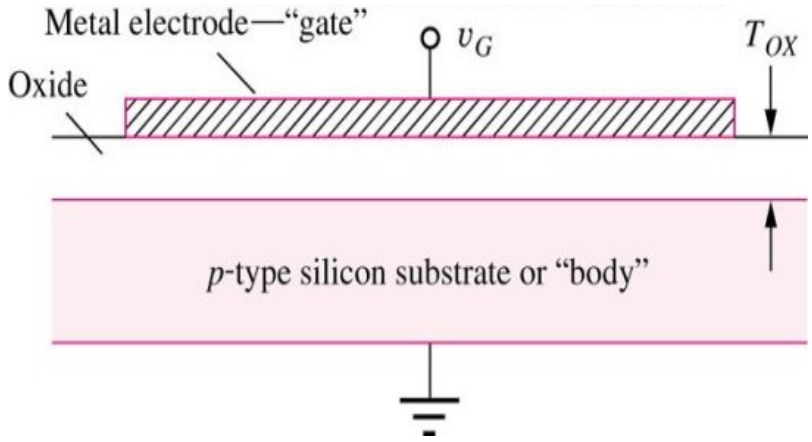
# FACULTY OF ENGINEERING AND TECHNOLOGY

## MEC-022

## Lecture - 04

# MOS Capacitor Structure

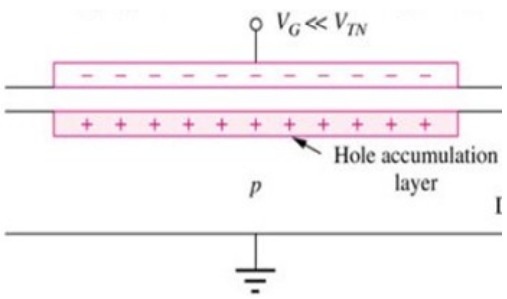
- Metal Oxide Semiconductor capacitor is the core structure of the a Metal Oxide Semiconductor Field Effect Transistor.
- Consists of two electrodes and insulator in between.
- First electrode (Gate): low-resistivity material such as metal or polycrystalline silicon.
- Dielectric - Silicon dioxide: stable high-quality electrical insulator between gate and substrate.
- Second electrode (Substrate, Body): *n*- or *p*-type semiconductor.
- The semiconductor body has limited supply of holes and electrons, and substantial resistivity.




The concentration of carriers being dependant on voltage, the capacitance of this structure therefore is a nonlinear function of voltage applied.

# Substrate Conditions for Different Biases

We consider the conditions of the semiconductor region (*p*-type) below the gate electrode under three different voltage bias: accumulation, depletion, inversion. Those conditions are determined by $V_{TN}$ (0.5 - 2.0 V) the threshold voltage, at which the electron inversion layer is just starting to form.




- **Accumulation :** $V_G << V_{TN}$

  The majority carriers (holes) accumulate in a very thin layer below the negative gate (like in capacitor)

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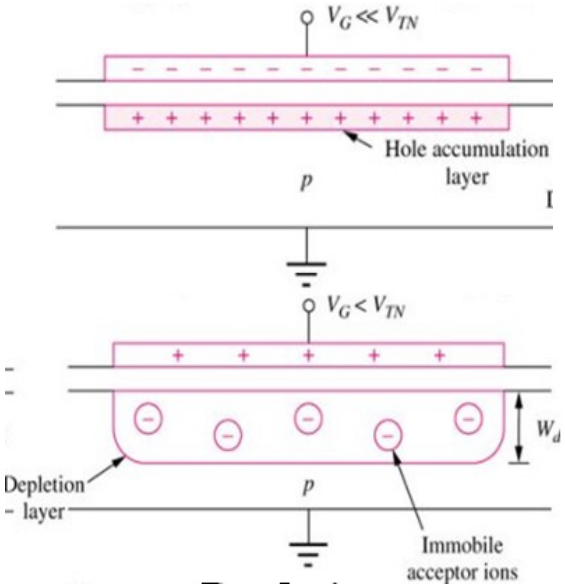


- **Accumulation :** $V_G << V_{TN}$ , $V_G < 0$

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- **Depletion:** $0 < V_G < V_{TN}$

  The small positive charge of the gate wipe out the holes from the layer below (depletes free carriers) creative a negative charge of ionized atoms

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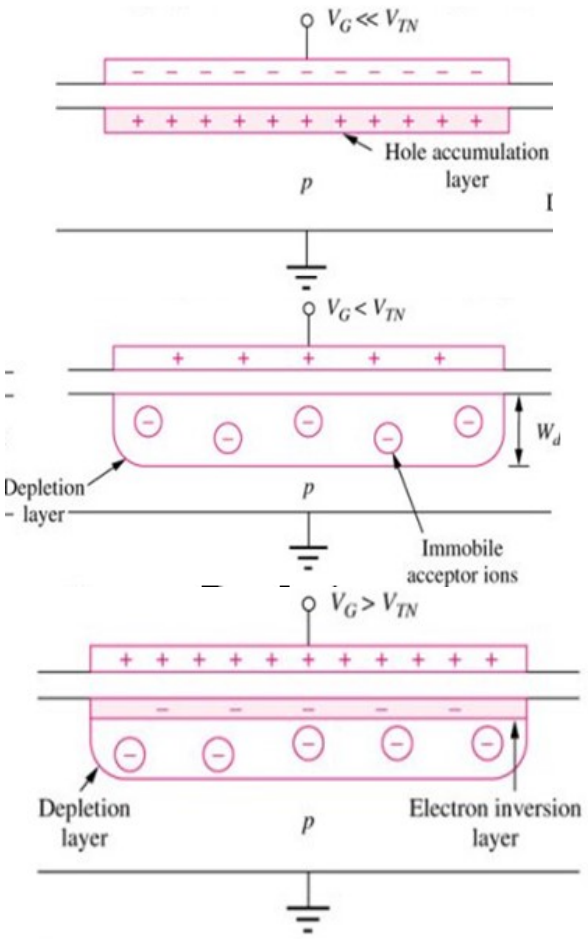


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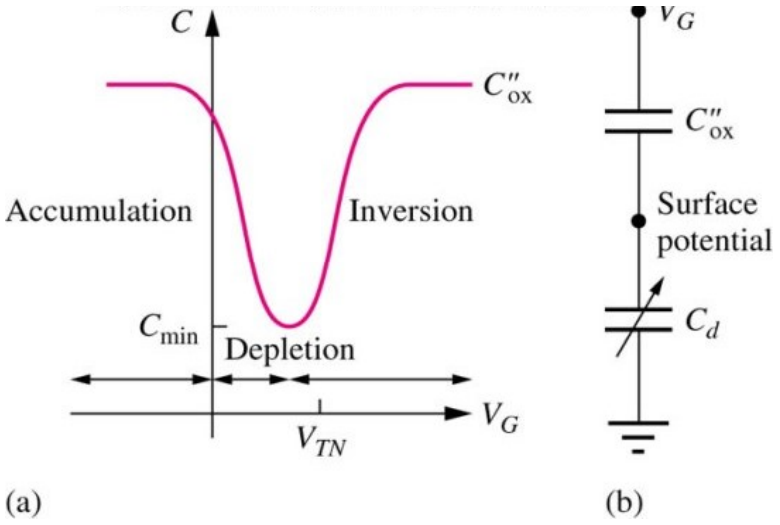
- **Inversion:** $V_G > V_{TN}$
  The larger positive charge of the gate attracts electrons whose concentration in the very thin layer exceeds that of holes – inversion of p-type into n-type.

# Low-frequency C-V Characteristics for MOS Capacitor on P-type Substrate




- MOS capacitance is non-linear function of voltage.
- Total capacitance in any region is dictated by the separation between capacitor plates.
- Total capacitance can be modeled as series combination of **fixed** oxide capacitance and **voltage-dependent** depletion layer capacitance.

$$C_{MOS,depletion} = A \bullet C_{depletion} = A \bullet \frac{C_{ox} C_D}{C_{ox} + C_D}$$


Thank You!